DETAILED PROJECT REPORT

On

CHIPS TO STARTUP (C2S) PROGRAMME

Microelectronics Development Division
R&D in Electronics Group
Ministry of Electronics & Information Technology
Government of India

सत्यमेव जयते

Contents

Preamble

To position India as a global hub for Electronics System Design and Manufacturing (ESDM) by encouraging the driving capabilities in the Country, Ministry of Electronics and Information Technology has come out with National Policy on Electronics 2019 (NPE-2019) for developing core components including chipsets and creating an enabling environment for the industry to compete globally. One of the main objectives of National Policy on Electronics 2019 is to Strengthen and leverage the existing manufacturing, research, design and development hubs for promoting design and innovation in the field of Electronics by working closely with Government, Industry, Academia, Universities and other Institutions of learning to design programme ensuring availability of adequate skilled manpower to the industry.

VLSI Design activity is one of the key areas of Microelectronics. This activity is knowledge intensive as well as capital intensive as it requires relatively less investment as compared to other areas of Microelectronics which is capital intensive. The knowledge-based industry such as VLSI Design, Embedded Design etc. leverages the skills of professionals for its growth & expansion. The fastest growing Indian software sector also needs VLSI design and embedded design professionals for moving up the value chain necessary for both accelerating and maintaining the growth rate. National Policy on Electronics 2019 also emphasizes on creating a globally competitive Electronic Design and Manufacturing Industry to meet the Country's need and to serve the international market by focusing on skills, technology and scale. In order to fulfill the vision and mission of NPE-2019, there is a fundamental need to create highly skilled and trained manpower in the areas of VLSI design and Embedded system by developing IPs/ASICs/SoCs/Systems for targeted applications through collaborative projects with Academia/R&D Organizations/Start-ups/MSMEs/Industries.

Special Manpower Development Programme for Chips to System Design (SMDP-C2SD) has already inculcated the culture of development of Working Prototypes of SoCs/ Systems /Sub-systems in the Academic / Research Institutes with identified Societal applications. To move up in the value chain and in order to fulfil the vision and mission of NPE-2019, there is a strong need to involve Industry(s) / Start-up(s) / MSMEs/ Incubate(s) / End user(s) (strategic / non-strategic) as part of SMDP Programme for design and development of users oriented, field trialled, deployable and re-usable IPs / SoCs / ASICs / Systems in addition to Specialized Manpower generation for Industry.

The proposed umbrella Programme "Chips to Startup (C2S)" not only aims at generating specialized manpower in the area of VLSI Design and Embedded System but also inculcating the culture of entrepreneurship in related areas by way of facilitating translational research in collaboration with Industry/Start-ups etc.

Background

1.1 Initiation of SMDP Phase-I

During the 9th Plan, MeitY had initiated the project entitled **"Special Manpower Development Programme in VLSI Design and Related Software (SMDP-I)"** in Year 1998 with a view to increase India's share of the Global VLSI Design market from 0.5% to 5% by end of the 9th Plan period by making available specialized manpower required by the Design Centers / Industry. (SMDP- Phase-I) was implemented at 19 Academic and Research Institutions categorised into Resource Centres (7 in number - 5 IITs, IISc, CEERI) and Participating Institutes (12 in number) with a total outlay of Rs. 14.99 Crores. This programme resulted in generating about 9300 trained personnel with hands-on experience in VLSI design and related areas.

The following were the main activities undertaken during the Phase-I of the Special Manpower Development programme in VLSI Design and related Software:

i. **Instruction Enhancement Programme-**These programmes were for the faculty of Participating Institutions in selected topics of Microelectronics and related areas. The Programmes were typically of one week duration.

ii. **Training Laboratory Technicians** –The aim of this activity was to train the laboratory technicians on the hardware and software tools given under the program to the institutions so that they can be efficiently installed and effectively used by the students of the institutes.

iii. **Setting up of VLSI Design Laboratories-**VLSI Designing is one of the most important activities of Microelectronics. To promote Microelectronics in the country efforts had to be made to bring out the 'VLSI Design' culture in the country. It was with this view that Design Laboratories were set up with Electronic Design Automation (EDA) tools for design of VLSI circuits and appropriate hardware. These labs thus became the 'Fabless Design Centres' where the students could design the circuits.

iv. **Development of Learning Material (LMs) on various topics of VLSI and related software –** The main aim of this activity was to make available quality learning material on core subjects of Microelectronics / VLSI Design to faculty and students of the participating institutions.

v. Teaching of various courses on VLSI Design and related software at:

- B.Tech /B.E. Level (Type-IV Manpower)
- M.E. / M.Tech level in areas of Electronics, Communications, Computer Science, Instrumentation etc. (Type-III Manpower)
- M.E. / M.Tech in VLSI Design and Microelectronics (Type-II Manpower)

- PhD on different aspects of VLSI Design and Related Software (Type-I Manpower)

The aim here was to offer Microelectronics / VLSI courses to the students of institutes so that they could take up design projects / carry out research in this area.

1.2 Continuation of Programme in Tenth Plan: Initiation of SMDP Phase-II

The Phase II of the **Special Manpower Development Programme in VLSI design and related software (SMDP II)** was initiated in 2005 during the 10th Plan as a continuation of Phase I with the aim of consolidating the efforts that were made during the 9th Plan for generation of trained manpower required for VLSI design. The Phase II of the SMDP project brought additional participating institutions under its purview making the total number of implementing organisations to 32 with total outlay of Rs. 49.98 Crores and duration of 5 years which was later extended by three more years. Under SMDP-II, a total of 28,170 engineering graduates in Electronics/ Communication/ Computer Science/ Instrumentation etc. had taken a graduate level course in VLSI design. At post graduate level, 6,439 students had taken at least two courses in various aspects of VLSI Design and CAD. An additional 3,924 post graduate students had their specialization at ME/M. Tech in VLSI design & CAD. Further 402 PhDs in various aspects of VLSI design & CAD were enrolled/ generated.

The following were the objectives of the programme:

- **Primary Objective -**To train special manpower in the area of VLSI Design and related software at M.E./M.Tech level (Type-II manpower). In addition to this, generation of Type-III manpower i.e. M.E./M.Tech in other areas of electronics etc. with at least two courses on VLSI design will also be undertaken.

- **Secondary Objective -** To train Type-IV manpower i.e. B.E/B. Tech in Electronics etc. with graduate level courses on VLSI Design. However, the program will not only be limited to generation of Type-II, III & IV manpower but would endeavour to generate PhD in various aspects of VLSI design/microelectronics (Type-I manpower) manpower as well. The establishment of VLSI design laboratories at all the 32 intuitions would also strengthen their academic program.

1.2.1 Major elements of the Programme were

i. Establishing State –of-the art VLSI Design Laboratory.
ii. Generation of manpower in VLSI Design area at various levels.
iii. Instruction Enhancement Program (IEP) for Faculty of PIs.
iv. Workshop involving International Guest Faculty.
v. India Chip Program.
vi. National VLSI website and 7 sites at RCs.

Date of Initiation: 21.03.2005

Date of Completion: 31.03. 2013

Total Outlay Rs.49.98 Crores

1.2.2 Implementing Institutions

7 Resource Centres (including 5 IITs, IISc Bangalore and CEERI Pilani) and 25 Participating Institutes (including 17 NITs and 8 other Institutions). The 32 institutions that supported as Resource Centres & Participating Institutions in Special Manpower Development Programme for VLSI Design and Related Software (Phase-II) are listed below in Table 1.1.

Table 1.1: Institutions under SMDP Phase-II

7 Resource Centers
25 Participating Institutions Association

IIT-Delhi 1. NIT Srinagar* 2. NIT Hamirpur* 3. NIT Jalandhar* 4. IIT Guwahati*		**IISc-Bangalore** 1. NIT Surathkal 2. PSGCS&T Coimbatore 3. BESU Shibpur
IIT-Kharagpur 1. NIT Rourkela 2. *NIT Jamshedpur** 3. NIT Silchar* 4. Jadavpur Univ.	**IIT-Bombay** 1. NIT Surat* 2. NIT Bhopal* 3. NIT Nagpur 4. SGSITS Indore	**IIT-Madras** 1. NIT Trichy* 2. NIT Calicut* 3. NIT Warangal
IIT-Kanpur 1. NIT Allahabad* 2. NIT Durgapur* 3. *IIT Roorkee* 4. IT-BHU Banaras		**CEERI Pilani** 1. NIT Kurukshetra* 2. NIT Jaipur 3. TU Patiala

*** Institutions not in SMDP phase-I (Numbers = 13)**

1.2.3 Achievements against Major Elements of the Programme

1.2.3.1 Establishing State–of-the art VLSI Design Laboratory

VLSI Design Laboratories were established at 32 institutions equipped with State-of-the-art Hardware platforms and Electronic Design Automation (EDA) Tools. These Labs were being used by students at various levels (B.Tech / M.Tech / PhD) to undertake design of VLSI circuits. The details of the Hardware and EDA Tools are given in the Table 1.2 below.

Table 1.2: Hardware and EDA Tools

At RCs			
Hardware Details	**Quantity**	**EDA Tools**	**Licenses**
High end PC Servers	6 Nos	Cadence Tools Bundle	10 licenses
PC P4 based	14 Nos	Synopsys Tools Bundle	5 licenses
Printer, Scanner	1 No. each	Magma Tools Bundle	10 licenses
Associated networking		Mentor Tools Bundle	50 licenses
UPS – 15 KVA	1 Nos.	CoWare Tools	5 licenses
		Xilinx	
At PIs			
Hardware Details	**Quantity**	**EDA Tools**	**Licenses**
High end PC Servers	3 Nos	Cadence Tools Bundle	10 licenses
PC (P4 based)	9 Nos	Synopsys Tools Bundle	5 licenses
Printer	1 No.	Magma Tools Bundle	5 licenses
Associated networking		Mentor Tools Bundle	50 licenses
UPS – 15 KVA	1 No.	CoWare Tools	5 licenses
		Xilinx	

1.2.3.2 Generation of manpower in VLSI Design area at various levels

Under the Programme, the students of RCs and PIs at various levels such as B.Tech, M.Tech and Ph.D where introduced to specialized topics in VLSI Design. A model curriculum was also developed and adopted by the Institutions. The primary target of the Programme was to generate substantial number of manpower at M.Tech level having VLSI design as their primary specialization. B.Tech level as well as M.Tech Students in other areas also undertook courses (as electives) in VLSI and Microelectronics. The manpower generated under this programme at various levels is depicted in the Table 1.3 and in Fig. 1.1 below:

Table 1.3: Generated Manpower

Academic Year	2005-06	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13	Total
Type- I	24	40	29	49	54	49	67	90	**402**
Type -II	301	339	442	456	613	550	601	622	**3924**
Type-III	564	680	739	717	809	886	980	1064	**6439**
Type-IV	2445	2773	3285	3845	3889	3867	3798	4268	**28170**
Total	**3334**	**3832**	**4495**	**5067**	**5365**	**5352**	**5446**	**6044**	
Type-I: PhD. Type-II:ME/M.Tech (VLSI), Type-III: ME/M.Tech, Type-IV: BE/B.Tech.									

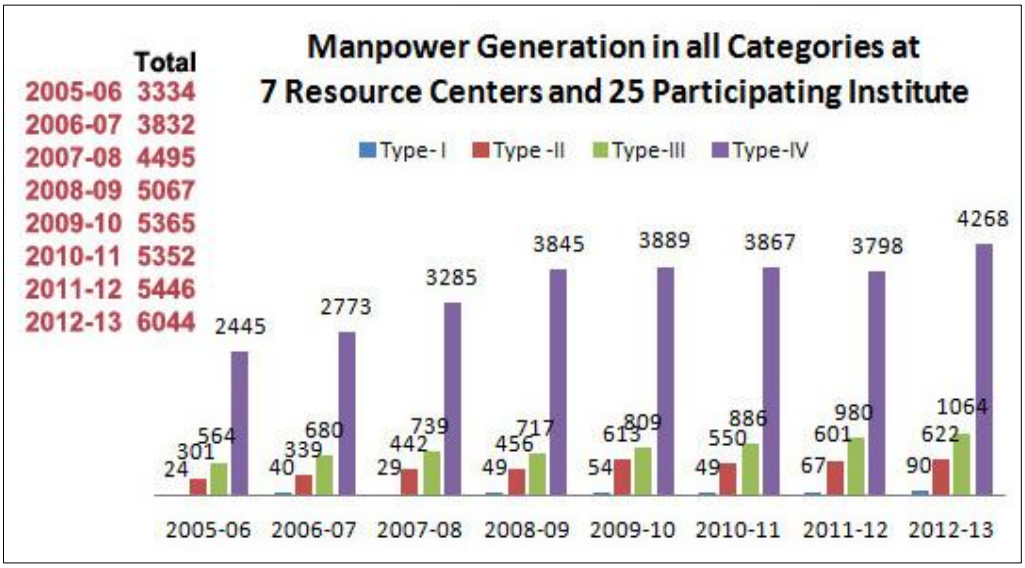


Fig. 1.1: Types of Manpower Generated

1.2.3.3 Instruction Enhancement Program (IEP) for faculties of PIs

23 Instruction Enhancement Programmes (IEPs) on different topics/areas were conducted at various RC/PI locations by Resource Centres for training faculty of Participating Institutions. A total of 654 faculties/Lab Engineers of PIs were trained through this programme. Details of various IEPs conducted are listed in the Table 1.4 below.

Table 1.4: Various IEPs conducted and number of participants

#	Topic	Name of the Institute	Date	No. of participants attended
1.	Digital IC Design	IIT Kanpur	July 3-14, 2006	21
2.	Low Power VLSI Design	IIT Kharagpur	Sep. 11-23, 2006	24
3.	RF IC Design	IIT Madras	Nov. 13-24, 2006	27
4.	Semiconductor Device Modelling& Simulation	IISc Bangalore	Dec. 4-15, 2006	18
5.	Analog IC Design	IIT Delhi	July 2-13, 2007	27
6.	VLSI-DSP Based Design	IIT Kharagpur	Sep. 24-Oct 05, 2007	27
7.	Synthesis of Digital System	IIT Kanpur	Dec. 10-21, 2007	25
8.	VLSI Testing & Verification	IISc Bangalore	Mar. 10-19,2008	24
9.	Technology CAD	IIT Kharagpur	May 12-17,2008	11
10.	Linux System Administration and EDA Tools Installation	CEERI Pilani	Oct. 14-18, 2008	26
11.	Mixed-Signal VLSI Design	IIT-Bombay	March 16-21, 2009	33
12.	FPGA Laboratory	IIT Delhi	July 13-18,2009	15
13.	System Modeling Using System C/VHDL/Verilog	CEERI Pilani	Dec. 14-23,2009	17
14.	Algorithms to Architectures	IIT Madras	Feb. 22-26,2010	17
15.	Low-Power, High Speed Digital Subsystem Design : Spec to Test	IIT Kharagpur	March 2-13,2010	14

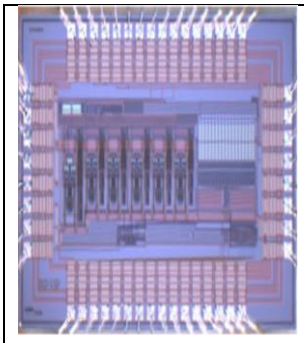
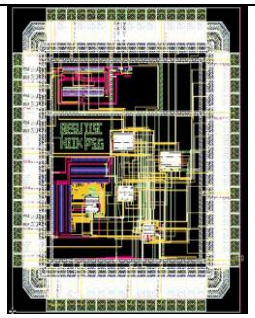
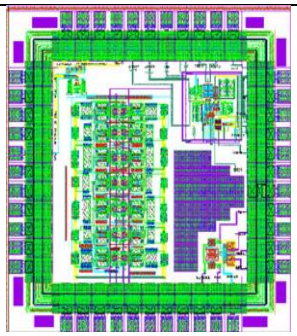
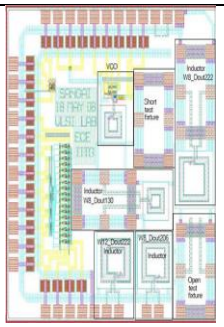
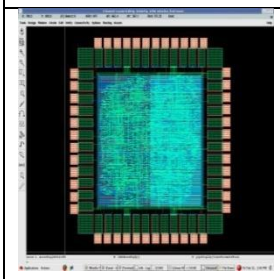
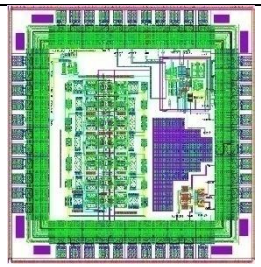
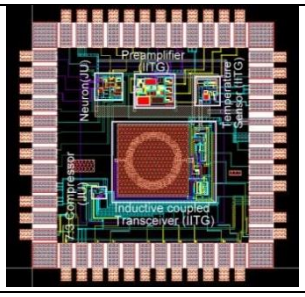
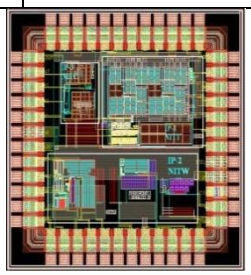
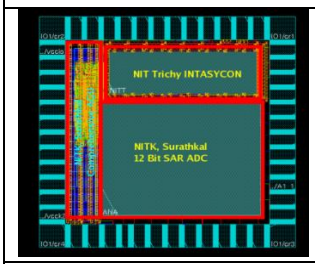
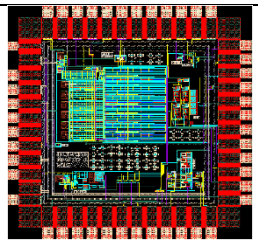
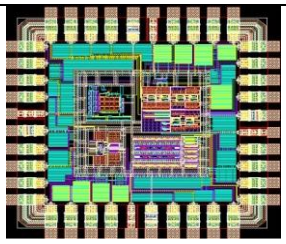
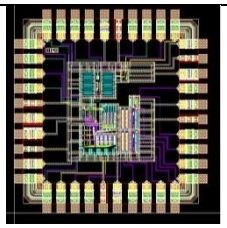
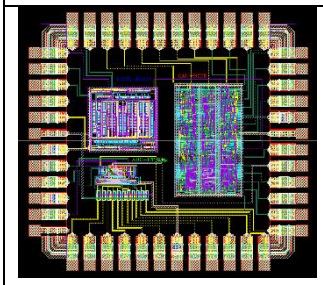
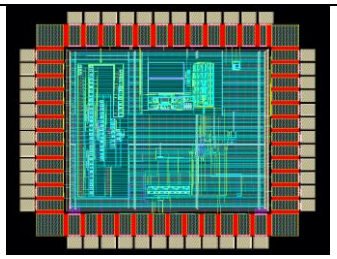
16.	Chip Integration and Tape out Issues	IIT Madras	Sept.29-Oct.2nd,2010	27
17.	Semiconductor Memory Design & Test	CEERI Pilani	Dec.13- 17, 2010	52
18	VLSI aspects on Biomedical Engineering	IIT Kharagpur	March 06-12,2011	22
19.	Low Noise Low Power OP Amp Design and Testing	IIT Delhi	March 14^{th} – 19^{th}, 2011	25
20.	India Chip: Chip finishing workshop	IIT Bombay	Oct. 8^{th} – 10^{th} ,2011	25
21.	Analog/Mixed Signal Design	IIT Madras, IISc. Bangalore IIT Delhi	Dec. 9^{th} – 12^{th} ,2011	~60
22.	RFIC & System Design	IIT Delhi	Jan 20, 2012	~20
23.	Low Power Digital Design	IIT Kanpur	Sept. 24-28, 2012	21

1.2.3.4 India Chip Program

Fabrication of fourteen chips, 5 in single mode and 9 in "Multi Project Wafer (MPW)" mode were undertaken for Siliconization of Analog and Digital designs done by students of various RCs and PIs. In the five single mode design - IIT D prototyped 2 individuals designs whereas each of IIT M, IIT G and IIT Kharagpur prototyped single designs. For the design undertaken by IIT Kharagpur sub blocks were designed by NIT Durgapur, Jadavpur University and IIT Kharagpur itself.

In the MPW chips, 32 designs from 16 institutions were integrated together and were prototyped in nine chips. Seven institutions merged these 32 designs in 9 chips for Siliconization which acted like an integrator to merge the designs received from other institutions. In this way there was considerable savings in the fabrication cost. The institutions, which carried out the integration/merging of designs were, IISc Bangalore, IIT Guwahati, NIT Tiruchirapalli, IIT Kanpur, NIT Surathkal, VNIT Nagpur and IIT Kharagpur.

In addition to this, one MPW design was also carried out by IIEST Shibpur which had integrated designs from IIT Kharagpur, NIT Rourkela and IIEST Shibpur. This design was fabricated at Euro practice. Another MPW integrating designs obtained from MANIT Bhopal, MNNIT Allahabad, NIT Hamirpur, MNIT Jaipur, NIT Jalandhar, NIT Kurukshetra, NIT Silchar, CEERI Pilani were integrated by MeitY and submitted for fabrication at Euro practice by CEERI Pilani. The packaged chips received after fabrications were tested by the respective institutions. The details of all the MPW designs undertaken are shown in Table 1.5 below.

			
Mixed Signal Design from IIT Madras	Analog & Digital Design: Integrating Design from four institutions	Analog Design from IIT Delhi	Analog & Digital Design from IIT Guwahati
			
Digital Design: Integrating designs from 5 institutions	Analog Design from IIT-Delhi	Analog Design: Integrating designs from 2 institutions	Analog Design: Integrating designs from 3 institutions
			
Digital Design: Integrating designs from 2 institutions	Analog Design: Integrating designs from 6 institutions	Analog & Digital Design from IIT-Kgp	Analog &Digital Design: Integrating designs from three institutions.
	BESU Shibpur NIT Rourkela IIT Kharagpur		MNNIT Allahabad, MANIT Bhopal, CEERI Pilani, DEITY Delhi, NIT Hamirpur, MNIT Jaipur, NIT Jalandhar, NIT Kurukshetra, NIT Silchar
Transistor Level S-Box Design for Efficient Implementation of the AES IC Implementation of Control Area Network (CAN) ADC.		ADC,Key board decoder circuit for microcontroller interface, Adder, Hamming Code Decoder, Differential amplifier, Parity Generator	

Design
1-Bit A
6-BIT I
10-Bit S
4x4 key

Table 1.5: Chip Layout views of integrated designs under India Chip Programme

1.2.3.5 Workshop involving International Guest Faculty

The workshops on Recent Advances in Analog VLSI Design; Technology and Application of Medical Imaging; VLSI Interconnects & Signal Integrity; and Cognitive Radio and CMOS RF Circuit and System challenges were organized at various RC locations during January 11-18, 2007, January 03-16, 2011, November 25-December 15, 2011 and January 09-20, 2012 respectively. In these workshops, Prof. W.A Serdijn, from Technical University Delft Netherlands, Dr. Rajiv Gupta from Massachusetts General Hospital/Harvard Medical School, Prof. Ram Achar from Carleton University, Ottawa, Ontario and Prof. Eric Klumperink from University of Twente were invited to give series of lectures on the current area of research. The details of the workshops conducted involving international guest faculty/number of participants in these workshops is given in table 1.6 below.

Table 1.6: Workshops Conducted

Name of Invited Guest Faculty	Period	Topic	Location
Prof. Wouter A. Serdijn Delft University	January 11-18 , 2007	Recent Advances in Low- Power, Low Voltage Analog Designs and Ultra –wide band Transceivers	IIT Kharagpur IIT Delhi IIT Madras
Dr. Rajiv Gupta. Harvard Medical School	January 03-16, 2010	Technology and Application of Medical Imaging	IIT Kharagpur IIT Delhi IIT Bombay CEERI + BITS
Prof. Ram Achar. Carleton University	November 25 - December 15 , 2011	Fundamental & Advances in VLSI Interconnects & Signal Integrity	IIT Delhi CEERI Pilani IIT Kharagpur IIT Bombay IISc. Bangalore NIT Surathkal PSGCT Coimbatore
Prof. Eric Klumperink University of Twente	January 09-20, 2012	• Cognitive Radio and CMOS RF Circuit and System challenges. • Wideband Receivers exploiting thermal Noise Canceling. • Advances in low jitter CMOS clock generation. • CMOS Frequency Translation Circuits	IISc. Bangalore IIT Madras IIT Bombay IIT Delhi

1.2.3.6 National VLSI website and 7 sites at RCs

The seven Resource Centres had established individual websites to disseminate information connected with VLSI design. A centralized website (http://www.smdp2vlsi.gov.in) was also established at DeitY which acted as a repository of all information and facilitated its access to institutions which were not covered under SMDP-II. The model curriculum developed, lecture materials for all the IEPs held were made available through this website. The URL of the website created for SMDP-II by various centres is given below.

- IIT Bombay: http://www.ee.iitb.ac.in/~smdp/
- IIT Madras: http://www.ee.iitm.ac.in/vlsi/start

- IIT Kanpur: http://www.iitk.ac.in/vlsi/
- IIT Kharagpur: http://www.smdp.iitkgp.ernet.in/
- IISc. Bangalore: http://www.cedt.iisc.ernet.in/smdp/
- CEERI Pilani: http://idg.ceeri.ernet.in/smdp2.html
- IIT Delhi: http://web.iitd.ac.in/~ee/~iec/smdp.html

1.2.3.7 Other Activities Undertaken in SMDP-II

i. "Best M.Tech Thesis Award" was awarded to RCs & PIs during the three consecutive years (2007-08, 2008-09, and 2009-10). The details of these are given in the table 1.7 below.

Table 1.7: Best M.Tech Thesis awards under the programme

Resource Centres	
FY 2007-08	First Prize: "Adaptive Keeper Design for Dynamic Logic Circuits Using Rate Sensing Technique" IISc. Bangalore
	Second Prize : "Design of an Analog VLSI Chip to emulate Directional an d Orientation Selectivity in Visual Cortex" IIT Delhi
FY 2008-09	First Prize: "Low Power Design Techniques for the Front End of a Radio Frequency Communication Receiver" IISc. Bangalore
	Second Prize: "FPGA based Video Tracker" IIT Kharagpur
FY 2009-10	First Prize (Joint Award):1. "Non-Quasi Static Modelling of Multi-Gate MOSFETs" IISc. Bangalore.
	2. "Power and Performance Optimization Using Multi Voltage, Multi Threshold and Clock Gating" IIT Kanpur
Participating Institutes	
FY 2007-08	First Prize: "Design and Analysis of 12 Bit Segmented DAC" Thapar University
	Second Prize: "Design, Modelling & Simulation of MEMS Capacitive Shunt Switch and its Application as Phase Shifter for Ku Band" Jadavpur University
FY 2008-09	First Prize: "Design of Resolution Adaptive TIQ Flash ADC using AMS 0.35-micron Technology" NIT Surathkal
	Second Prize: "Design of Multi-band CMOS Low Noise Amplifier" IIT Guwahati
FY 2009-10	First Prize: "VLSI Architecture of Galois Field Arithmetic Circuit" IIEST Shibpur
	Second Prize: "Design of a 0.5 V Low Power Analog Front-End for Heart-rate Detector" IIT Guwahati

ii. Financial support was provided to attend 20 International conferences to Institutions participating in the SMDP-II project. The Table 1.8 given below summaries the support provided to various institutions.

Table 1.8: Support provided to attend International conferences

Name of the RC	Name of the PI	Name of Conference
IIT Kanpur -3 IIT Kharagpur -1 CEERI Pilani – 1 IIT Madras - 1	NIT Trichy - 2 NIT Calicut - 3 PSG - Coimbatore - 1 Thapar University Patiala - 1 MNIT Jaipur - 1 NIT Srinagar - 1 SGSIT Indore - 3 IIT Roorkee – 2	IEEE International conference on Field Programmable Technology , ICED – 2008 , 24th IEEE Norchip Conference , 24th IEEE Norchip Conference , IEEE ISCAS – 2006 , ICIIS -2007 , International Conference on Materials for Advanced Technologies 2007 , IMOC – 2007 , ISCAS – 2008, DATICS – 2009, IEEE IMEC-DATICS-2009, ICCS-2008,WCESCS 2008, TENCON-2009, IEEE computer Society Annual Symposium, IEEE Symposium on Computer and Informatics (ISCI 2011), IEEE International Conference on Electronic Devices, Systems & Applications (ICEDSA 2011), AUTOTESTCON 2011, IEEE NATW 2012 Woburn USA,ISCAS Seoul, Korea.

1.3 Continuation of Programme in Eleventh Plan: Initiation of SMDP-C2SD

During the 11th Plan, as a continuation of II Phase, 3rd Phase of the Special Manpower Development Programme (SMDP III) was conceptualized by MeitY with an aim not only to develop specialized manpower in VLSI Design but also to develop Working Prototype of System-on-Chip/ System/Sub-Systems using the ASICs/ICs developed in-house.

An umbrella Programme entitled **"Special Manpower Development Programme for Chips to System Design (SMDP-C2SD)"** was initiated under 'Digital India Programme' in December 2014 over a period of 5 years with total outlay of Rs. 99.72 Crore at 60 academic/ R&D institutions spread across the Country including IITs, NITs, IISc, IIITs & other Engineering Colleges with an aim to train 50,000 number of specialized manpower in the area of VLSI design and inculcate the culture of System-on-Chip (SoC)/ System Level Design at Bachelors, Masters and Research level. The Programme duration was later extended by 23 Months up to November, 2021.

The following were the objectives of the Special Manpower Development Programme for Chips to System Design:

- To bring in a culture of System on Chip / System designing by developing working prototypes with societal applications
- Capacity building in the area of VLSI/ microelectronics and Chip to System development.
- To broaden the base of ASIC / IC designing in the country
- To broaden the R&D base of Microelectronics / Chip to System through Networked PhD program
- To promote 'Knowledge Exchange Program'
- Protection of Intellectual Property generated

Date of Initiation: December 2014

Total Outlay: Rs. 99.72 Crore

Duration: 30th November 2021.

Implementing Institutions

The program is being implemented at 60 Institutions (including IITs, NITs, IISc, IIITs & other Engineering Colleges) spread across the country. There are 10 Resource Centres (RCs) which are the mentoring institutions for 50 Participating Institutions (PIs). The 60 Institutions participating in the program are listed below in Table 1.9.

Table 1.9: Institutions under SMDP-C2SD

Category I	Category II	Category III
10 Resource Centres	**Participating Institutions which were there in SMDP-II and New IITs(which were not earlier in SMDP-II) (30)**	**New Participating Institutions (20)**
1. IIT Kharagpur 2. IIT Bombay 3. IIT Madras 4. IIT Kanpur 5. IIT Delhi 6. IIT Guwahati 7. IIT Roorkee 8. IISc Bangalore 9. CEERI, Pilani 10. VNIT, Nagpur	**PIs which were there in SMDP-II** 11. NIT Srinagar 12. DBRANIT Jalandhar 13. NIT Hamirpur 14. NIT Kurukshetra 15. ThaparUniversity Patiala 16. MNIT Jaipur 17. MNNIT Allahabad 18. IIT(BHU) Varanasi 19. NIT Durgapur 20. NIT Silchar 21. IIEST Shibpur 22. PSG College of Technology, Coimbatore 23. NIT Jamshedpur 24. NIT Rourkela 25. NIT Warangal 26. NIT Surathkal 27. SVNIT Surat 28. MANIT Bhopal 29. SGSITS Indore 30. NIT Calicut 31. NIT Tiruchirappalli 32. Jadavpur University **New IITs** 33. IIT Mandi 34. IIT Ropar 35. IIT Jodhpur 36. IIT Bhubaneshwar 37. IIT Gandhinagar 38. IIT Indore 39. IIT Hyderabad 40. IIT Patna	41. NIT Agartala 42. NIT Patna 43. NIT Raipur 44. NIT Sikkim 45. NIT Goa 46. NIT Arunachal Pradesh 47. NIT Meghalaya 48. NIT Nagaland 49. NIT Manipur 50. NIT Mizoram 51. NIT Uttarakhand 52. NIT Delhi 53. NIT Puducherry 54. IIIT Allahabad 55. ABVIIITM Gwalior 56. PDPMIIIT(D&M) Jabalpur 57. IIIT(D&M) Kanchipuram 58. NIELIT Calicut 59. University of Calcutta 60. Indira Gandhi Technical University for Women, Delhi

1.3.1 Achievements against Major Elements of the SMDP-C2SD Programme

1.3.1.1 Development of Specialized Manpower in VLSI / SoC / System / Sub-System Designing

Under the programme, during first 5 Year of Programme, 52,365 no. of Industry ready Specialised Manpower has been generated in VLSI/ System Design Area at B.Tech, M.Tech and PhD level, which includes:

- Type-I (PhD)
- Type-II (M.Tech in VLSI),
- Type-III (M.Tech in Computer/ Communication etc. with at least two VLSI courses / minor project in VLSI)
- Type-IV (B.Tech with at least two VLSI Courses/ minor project in VLSI)

And other Students, who have utilized the VLSI Lab Resources created at Institutions under SMDP Programme.

The manpower generated under this programme at various levels is depicted in the Table 1.10 and in Fig. 1.2 below:

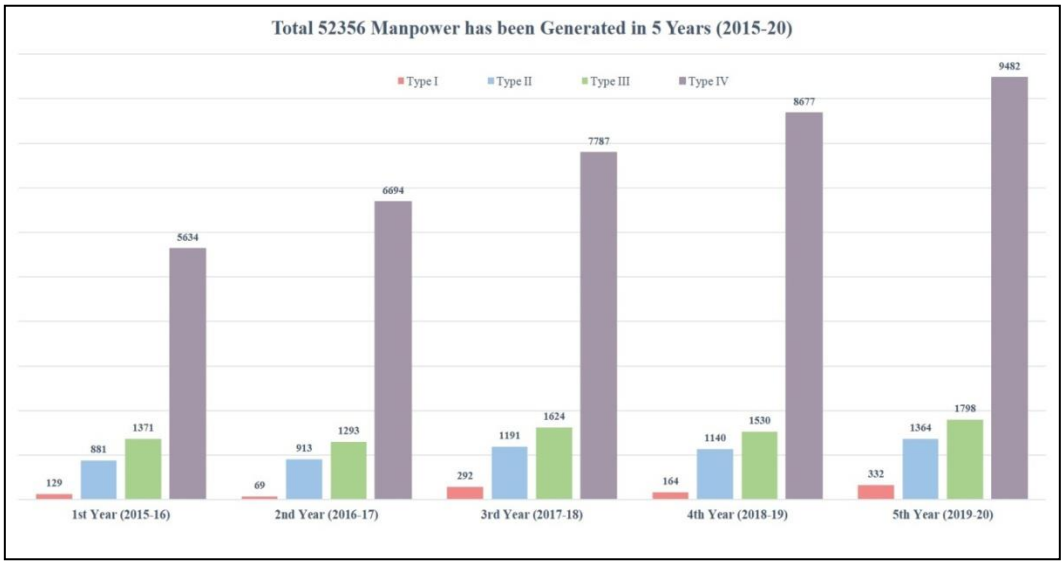


Fig. 1.2: Types of Manpower generated

#	1st Year (2015-16)	2nd Year (2016-17)	3rd Year (2017-18)	4th Year (2018-19)	5th Year (2019-20)	Total
Type I	129	69	292	164	332	986
Type II	881	913	1191	1140	1364	5419
Type III	1371	1293	1624	1530	1798	7556
Type IV	5634	6694	7787	8677	9482	38082
Total	**8015**	**8969**	**10894**	**11511**	**12976**	**52365**

Table 1.10: No of Manpower Generated

1.3.1.2 Establishing State–of-the art VLSI Design Laboratory

State-of-the-Art VLSI Design Laboratories were established at 60 Institutions equipped with Hardware platforms and Electronic Design Automation (EDA) Tools from Cadence/ Synopsys/ Mentor/ Xilinx. These labs are not only used by students involved under SMDP-C2SD project to undertake design of VLSI circuits but also by students from other Departments & nearby institutes.

1.3.1.3 Development of Working Prototype of Systems

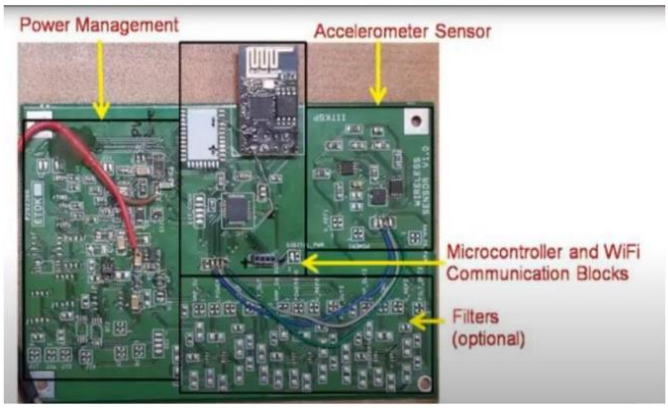
Under the programme, in order to inculcate the culture of Chip to System development activity at Institutions, 15 Systems/SoCs were undertaken by 10 RCs for development of Working Prototype. For each system project, End users were identified and specifications were finalized in consultation with them. The End users were also involved in the Project Review Committee for continuous monitoring of the Project. Systems developed under the Programme are listed below.

Table 1.11: System Developed under the Programme

#	System Project Title	RC	End User/ Application
1	ASIC for Next Generation LCA	IISc-B	ADA (DRDO) & ISRO
2	Integrated microchip module for wireless capsule endoscopy	IIT-D	Healthcare
3	Collision Detection in Automobiles using CMOS Imagers		Healthcare
4.	MAVI: Mobility Assistant for the Visually Impaired		Automotive
5.	Versatile Data Acquisition & Signal Processing Platform with specific emphasis on Seismic Application	IIT-Kgp	Disaster Management, MoES
6.	Design and Implementation of variable data rate (up to 10 GBPS) (SerDes Serializer/ Deserializer) system		ISRO and DRDO
7	Wireless Sensor Networks Node for Internet of Things (IoT)	VNIT-N	Railways
8	Versatile Physiological Signal Monitoring System	IIT-B	Healthcare
9	SerDes: High Speed Data Transceiver		SAC (ISRO)
10	Low Power Speech Recognition System using a custom IC	IIT-M	Consumer Electronics
11	UWB beam-forming Camera		Strategic
12	Wireless Sensor Node – System On Chip (WSN-SOC) for Monitoring of illegal activities	IIT-K	Forest Department of Odisha
13	RF Sensing of Cardiopulmonary Motion for survival detection under debris	IIT-R	NDRF Uttarakhand/ Disaster Management
14	System-on-Chip platform for Secured Speech Communication	CEERI	Strategic sector
15	FPGA/ASIC based Sensor Platform for Monitoring Air Pollutants	IIT-G	Assam Pollution Control Board

System Projects

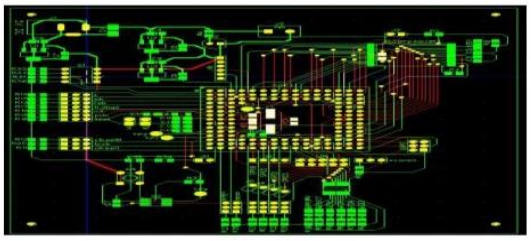
1 **Versatile Data Acquisition & Signal Processing Platform with specific emphasis on Seismic Application** is being designed by **IIT Kharagpur**. This system can generate the early warning within one second of P-Wave to save lives and property beyond 200 KM from the earth quake epicenter. After testing and field trials, the whole system will be deployed in earth quake detection centre installed at Sikkim funded by Ministry of Earth Science, Government of India.

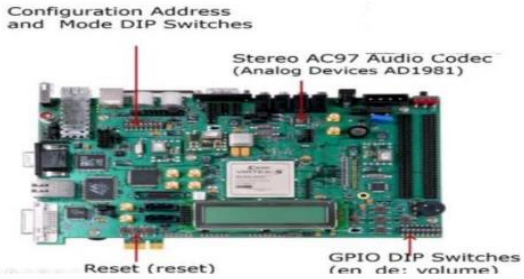


2 **IIT Kharagpur** has also developed **Serializer Deserializer (SerDes)** with data rate of 12.5 Gbps. The design is being explored by ISRO for usage in Satellite Launch vehicles and further enhancements as per their requirements. IITKGP is also in process of designing a SerDes with 20 Gbps data rate.

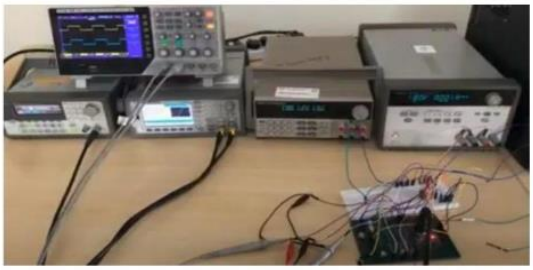
System Projects

3 The design, development and implementation of an open-source IP core based system-on-chip (SOC) design platform and its application to **Secure Speech Transmission & Reception** is in process by CEERI Pilani for Centre for Artificial Intelligence and Robotics (CAIR), DRDO. The sub-modules of the system like Vocoder, Cipher etc. are developed by **CEERI** in-house.

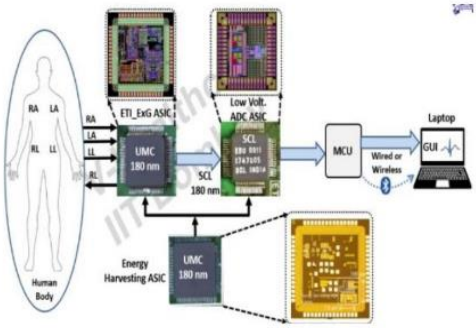




4 **IISc Bangalore** is developing a mixed signal ASIC for smart probe for **Next Generation LCA**. A Working prototype has been developed for Wireless Telemetry System with Energy Harvesting for Strategic Sectors: Probe for LCA (DRDO), Satellite Wiring Harness (ISRO), Launch Vehicle telemetry (ISRO). Close interaction with ADA, DRDO is in progress for incorporating their requirement in the System.

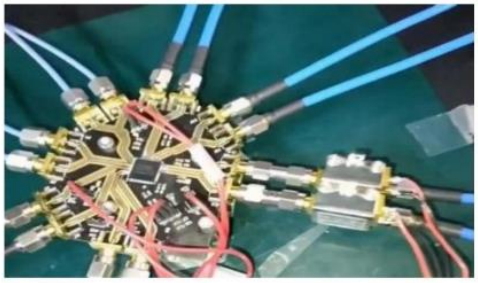


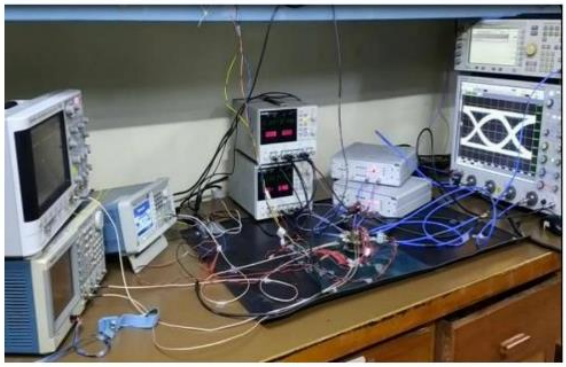
5 **A Versatile Physiological Signal Monitoring System for Healthcare** is being developed by **IIT Bombay**. A working Prototype has been developed for Versatile Physiological Signal Monitoring System using adaptive Artefact removal techniques.

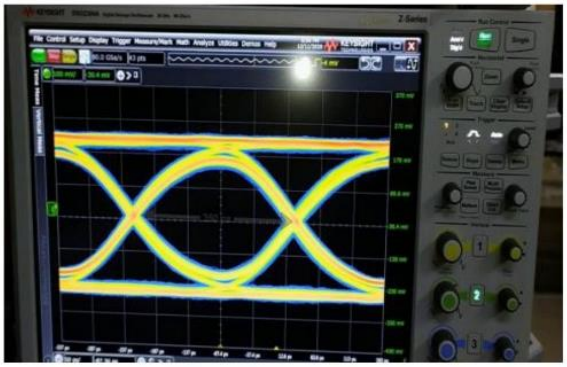


System Projects

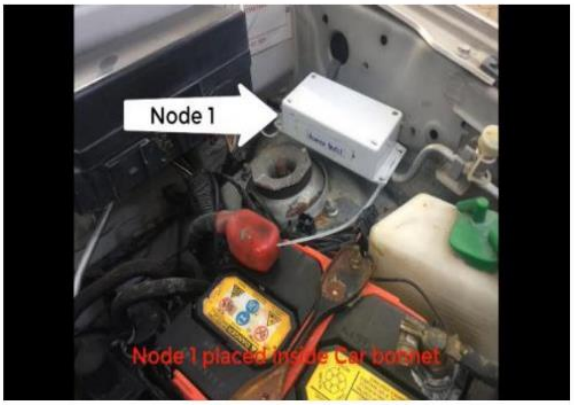
6 A **Serializer Deserializer** with high-speed serial links for module-to-module or chip-to-chip communication on board satellites is also being developed by **IIT Bombay**. SerDes with data rate of 16 GBPS has been designed and interaction with ISRO is in progress.





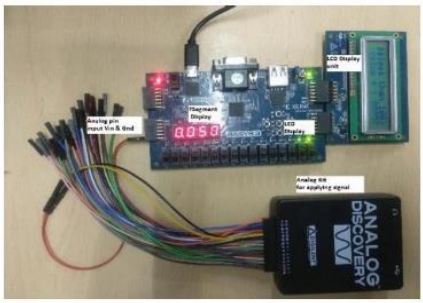


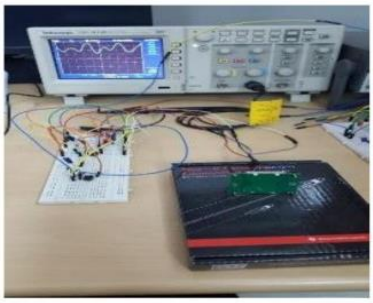
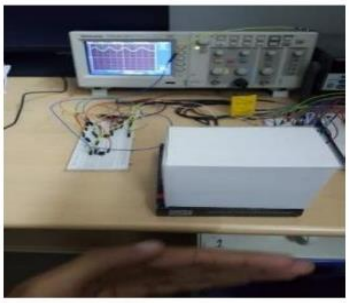
7 The design and development of **Wireless Sensor Node** at board level (COTS) and chip level with ZigBee standards is being developed by **VNIT Nagpur** for the use in Railways. A working prototype has been developed for WSN for Railway Stock Health Monitoring System. Field trials on the passenger train in Nagpur-Ramtek and on car with improved antenna characteristic have been conducted.



System Projects

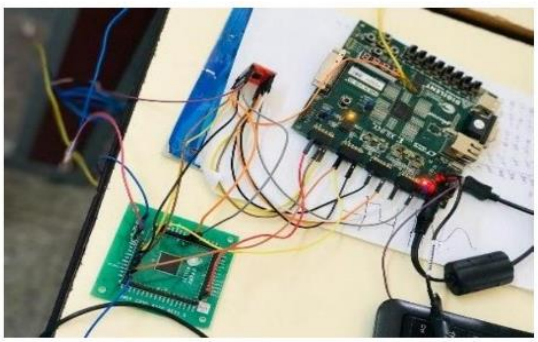
8 A system for **RF Sensing of Cardiopulmonary Motion for survival detection under debris** is being developed by **IIT Roorkee** with an aim to detect humans trapped under debris in disaster affected areas using RF sensing of cardiopulmonary motion. The system will be later adopted by National Disaster Response Board (NDRF) Uttarakhand, National Disaster Management Authority, Govt. of Uttarakhand.



9 An **On-chip Speech Recognition System** is being designed by **IIT Madras** with an aim to develop a standalone system for offline speech recognition with large language models with a primary interest as IP for embedded applications/SoCs.

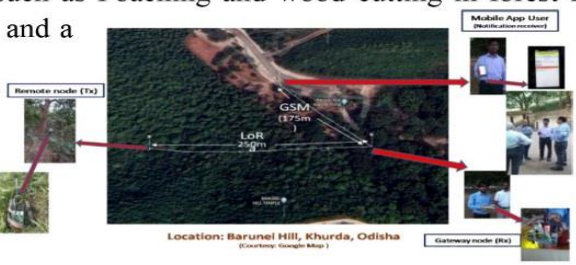

10 The design and development of an **Array Signal Processor ASIC** is being carried out by **IIT Madras** which will be used by Naval Physical and Oceanographic Laboratory (NPOL) DRDO, Kochi.

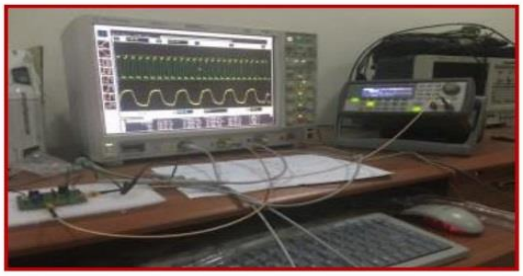



System Projects

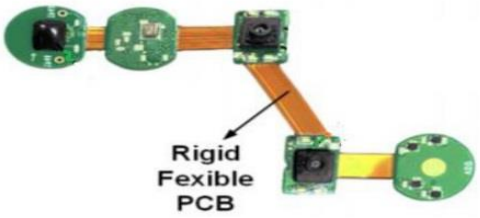
11 An **Air Quality Monitoring System (AQMS)** is being developed by **IIT Guwahati** which can sense harmful gases like CO_2, CO, NO_2 along with Temperature and Humidity sensing. Assam Pollution Control Board has been approached to adopt the system.

12 **Wireless Sensor Node - System On Chip (WSN-SOC)** for efficient sensing and monitoring of illegal activities such as Poaching and wood cutting in forest is being developed by **IIT Kanpur** and a working prototype has been developed for Gun-shot and Wood-cutting sound detection. The field trials have been carried out in the forests of Orissa. The system will be adopted by the Forest Department, Govt. of Orissa.





13 **IIT Delhi** is designing an integrated microchip module for **Wireless Capsule Endoscopy** for Healthcare users. This system is a complete imaging solution (a prototype solution, on a single chip) for transmission of compressed digestive tract images over a wireless link



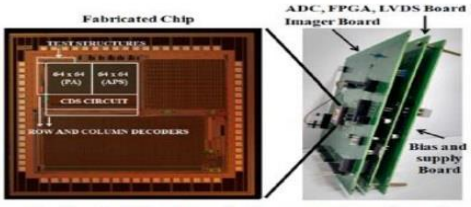
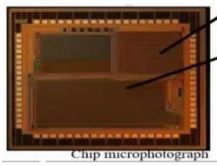


Figure 1: Fabricated sensor and test boards

System Projects

14 A **collision detector** for detection of obstacles and collision in Automobiles using CMOS Imagers is being developed by **IIT Delhi**. A Working prototype has been developed for Collision Detection using CMOS Imagers for parallel velocity/depth estimation, motion direction classification, and robustness to background light. Interest has been received from automotive industry to incorporate their requirement.

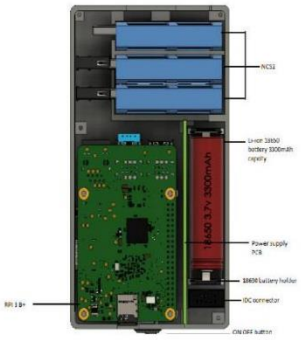


Chip microphotograph

Parameter	Values
Technology	AMS 0.35 µm OPTO process
Pixel pitch	48 µm
Fill factor	17.36 %
Array size	24 x 24

Parameter	Values
Technology	AMS 0.35 µm OPTO process
Pixel pitch	35 µm
Fill factor	19 %
Array size	32 x 64

15 **IIT Delhi** is also developing a system on **Mobility Assistant for Visually Impaired (MAVI)**. It is a device to aid mobility of visually impaired people and address the issues of safety (identify- digging, potholes and stray animals), navigation (guided movements) and social inclusion (Face detection and recognition). The system is capable of detecting and alerting presence of Dogs and Cows, Human faces + face recognition from a library, Signboards (English and/or Hindi) + reading them out. A Mobile App has been developed for the same.



1.3.1.4 Development of Applications Specific Integrated Circuits (ASICs) and board level designs using FPGAs

To provide the exposure of complete design cycle of Chip development, ASICs designs were also undertaken by Participating Institutions who were part of previous SMDP programmes. Some of the ASICs designed by the PIs were also used in the 15 Working Prototype SoCs/ Systems, being developed for Strategic & Societal sectors.Under the Programme, total 150 ASIC fabricated and being fabricated at SCL and outside foundry as depicted in Figure 1.3 below. Additionally, 30 FPGA based board level designs were also undertaken by Category III institutions.

Fig. 1.3: Total ASIC fabricated at SCL and outside foundry

1.3.1.5 Establishment of Chip Centre

For undertaking Siliconization of ASICs/Integrated Circuits designed by the Participating Institution, Chip Centre was established at C-DAC, Bangalore. Chip Centre is the nodal centre for integrating the designs received from Institutions and sending them for fabrication at SCL in MPW mode. Chip Centre also facilitated the Institutions for packaging of bare dies received from SCL. Under the Programme, through Chip Centre, 111 ASICs were fabricated

and being fabricated at SCL in MPW mode. Chip Centre has also prepared the Checklists and templates to streamline the process of chip tape out at participating Institutions.

1.3.1.6 India Chip Programme

Under India Chip programme, ASICs fabricated by the Participating Institutions were supported for fabrication at overseas foundries in different technology nodes. Under India Chip Programme, total 32 designs were fabricated at outside foundry as depicted in Figure-1.4.

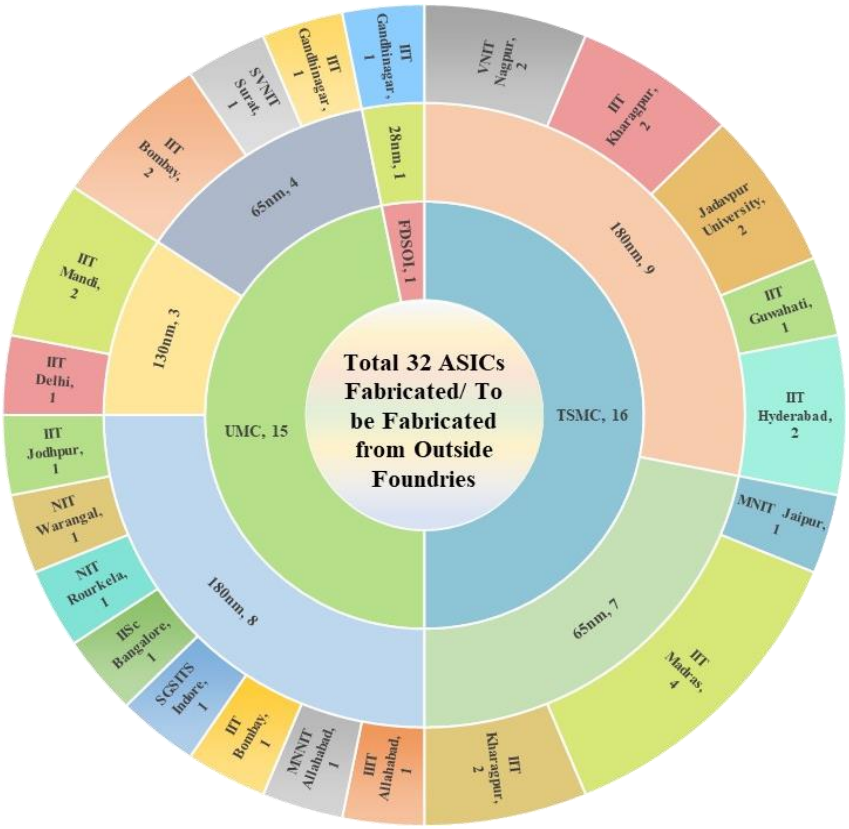


Fig. 1.4: Total ASIC fabricated at outside foundry

Also, for providing fabrication support to Institutions who were not the part of SMDP-C2SD programme, Request for Proposal announced at MeitY and SMDP-C2SD website for selecting 10 best designs per year for fabrication at SCL Mohali.

1.3.1.7 Instruction Enhancement Program (IEP) to enhance faculty expertise in Microelectronics & Chip to System

Under the programme, 15 Instruction Enhancement Programme (IEPs) on different topics/area were conducted at various RC/PI locations by RCs and PIs for training faculty of Participating Institutions. A total of 1885 faculties/Lab Engineers of PIs were trained through this IEP. Details of various IEPs conducted are listed in the Table 1.12 below:

Table 1.12: Conducted IEPs and number of participants

#	Institute	Date	Topic	Faculty/Student Attended
1.	IIT-D	7- 9 Dec' 15	System Level Design on Platform FPGAs	27
2.	IISc-B	4- 8 Jul' 16	Mixed Signal SOC: from design to tape out (.GDS2)	47
3.	IIT-B	11- 13 Jul' 16	Analog, Mixed-Signal and RF System Design	35
4.	VNIT-N	5- 9 Dec' 16	Design issues related to Deep Sub-Micron Technologies	35
5.	IIT-KGP/ IIT-Guwahati	10-14 Apr'17	Introduction to Analog & Digital VLSI Design	22
6.	IIT-KGP/ NIT-Sikkim	5-9 Jun' 17	Mixed Signal and RFIC Design	27
7.	IIT Madras	29Jan - 2 Feb' 18	Analog IC Design	25
8.	IIT Roorkee (with SCL Mohali)	24 - 29 Feb' 18	High Level Design to Silicon	60
9.	IIT Kharagpur	19- 23 Mar'18	IoT for Structural Health Monitoring	30
10.	CDAC Bangalore (Chip Centre)	10-14 June'19	PCB Design methodologies - a hands-on course	28
11.	IISc Bangalore	24-28 June'19	Mixed Signal SoC: from tape out to GDSII	49
12.	NIT Rourkela	1-5th July 19	Design Verification and Hardware Security	18
13.	IIEST Shibpur	26-3 0 Aug 19	Testing and Design-for-Testability for Digital Integrated Circuits	32
14.	NIELIT Calicut (Online training)	05-16 Oct 2020	Embedded System Design on FPGA covering Swadeshi Microprocessors	1000
15.		30 Nov- 12 Dec 2020	Embedded System Design on FPGA covering Swadeshi Microprocessors	450

1.3.1.8 Support for International Conference/Workshop outside

Under the programme, Researchers/Students of the 12 Participating institutions were supported for attending International Conferences and to present their work. Apart from this, 6 International Conference/Workshops were also supported in the area of VLSI/System under the programme.

Additionally, 5 ZoPP Workshop were conducted yearly for- reviewing the Project activities carried out by Institutions and working out Annual Action plan for all project implementing institutions & preparing Project Planning Matrix (PPM) for measuring the performance of the institutions.

Table 1.13: Support for attending International Conferences outside the Country

#	Institute Name	Conference Name	Year	Country	Duration
1	IIT Gandhinagar	Radiation and its Effects on Components and Systems (RADECS)	2016	Germany	19th-23th September
2	IIT Hyderabad	International Workshop on Signal Processing Systems(SiPS)	2017	Lorient, France	2nd - 5th October
3	Thapar University,Patiala	International Conference on Electrical and Electronics Engineering (ICEEE)	2017	Australia	2nd -3rd February
4	CEERI Pilani	International System-on-Chip Conference	2018	USA	4th -7th September
5	IIT-Bombay	International Symposium on Circuits and Systems (ISCAS)	2018	Florence, Italy	27th - 30th May
6	IIT Mandi	International Symposium on Circuits and Systems (ISCAS)	2018	ITALY	27th-30th May
7	IIT-Guwahati	International Microwave Symposium (IMS)	2019	Boston, USA	2nd -7th June
8	IIT-Bombay	International Symposium on Circuits & Systems (ISCAS)	2019	Japan	26th-29th May
9	Thapar University,Patiala	International Conference on Intelligent Systems (Intellisys)	2019	UK	5th -6th September
10	IIEST Shibpur	International Symposium on Devices, Circuits and Systems (ISDCS)	2019	Japan	6th -8th March
11	NIT Patna	International Symposium on Wireless Per sonal Multimedia Communication (WPMC-2019)	2019	Portugal	24th – 27th November
12	CEERI Pilani	International conference on trust privacy and security in Intelligent System and Application (IEEE TPS-ISA)	2019	California	12th – 14th December

Table 1.14: Support for Organizing International Conferences/Workshops in the Country

#	Institute Name	Conference Name	Year	Duration
1	IIT Roorkee	International Symposium on VLSI Design and Test (VDAT)	2017	29th -2nd July
2	C-DAC Bangalore	Analog VLSI & Mixed Signal Design	2017	15th-16th June
3	Thiagarajar College of Engineering, Madurai	International Symposium on VLSI Design and Test (VDAT)	2018	28th -30th June
4	IIT Indore	International Symposium on VLSI Design and Test (VDAT)	2019	4th - 6th July
5	IIT Goa	ARM Architecture and System-on-Chip (SoC) Design	2019	1st -3rd December
6	IIEST Shibpur	International Symposium on Devices, Circuits and System (ISDCS-2020)	2020	4th – 6th January

1.3.1.9 Patens/Publications

Under the Programme, 21 Patents have been filed by Participating Institutions in the area of VLSI/system design and about 1500 research papers published in reputed Conference Proceedings / Journals.

1.3.1.10 Developmentof Model Syllabus for B.Tech / M.Tech oriented towards SoC / System Designing and initiating M.Tech in VLSI / Embedded System Designing

With a view to promote System Designing in the country, a model syllabus / curriculum for B.Tech / M.Tech oriented towards SoC/ System Designing including practical works / minor projects etc. was prepared. The faculty of Resource Centres and other experts including experts from the industry was involved to work out the Model Syllabus. Efforts were made for adoption of this model syllabus curriculum oriented towards SoC / System Design in various institutions with the approval of their competent authorities which had facilitated the initiation of M.Tech in Microelectronics/VLSI design at 18 new participation institutions.

1.3.1.11 Involvement of Industry Associations and Experts

To ensure that the program deliverables meet the industry requirement, the industry experts involved at all the stages of the program. The experts were made members of the National Steering Committee (NSC), Technical Advisory Committee (TAC) and Project Review and Steering Group (PRSG). Also, experts from the industry were also involved in identification of SoC / system under the sub-activity ‘Chip to System Development’. Whereas students from SMDP-C2SD institutions sent to leading Semiconductor MNCs (Intel/ NXP/ Cadence/Synopsys & S.T.Microelectronics) for Internship of 6 months to 1 year duration throughout the programme.

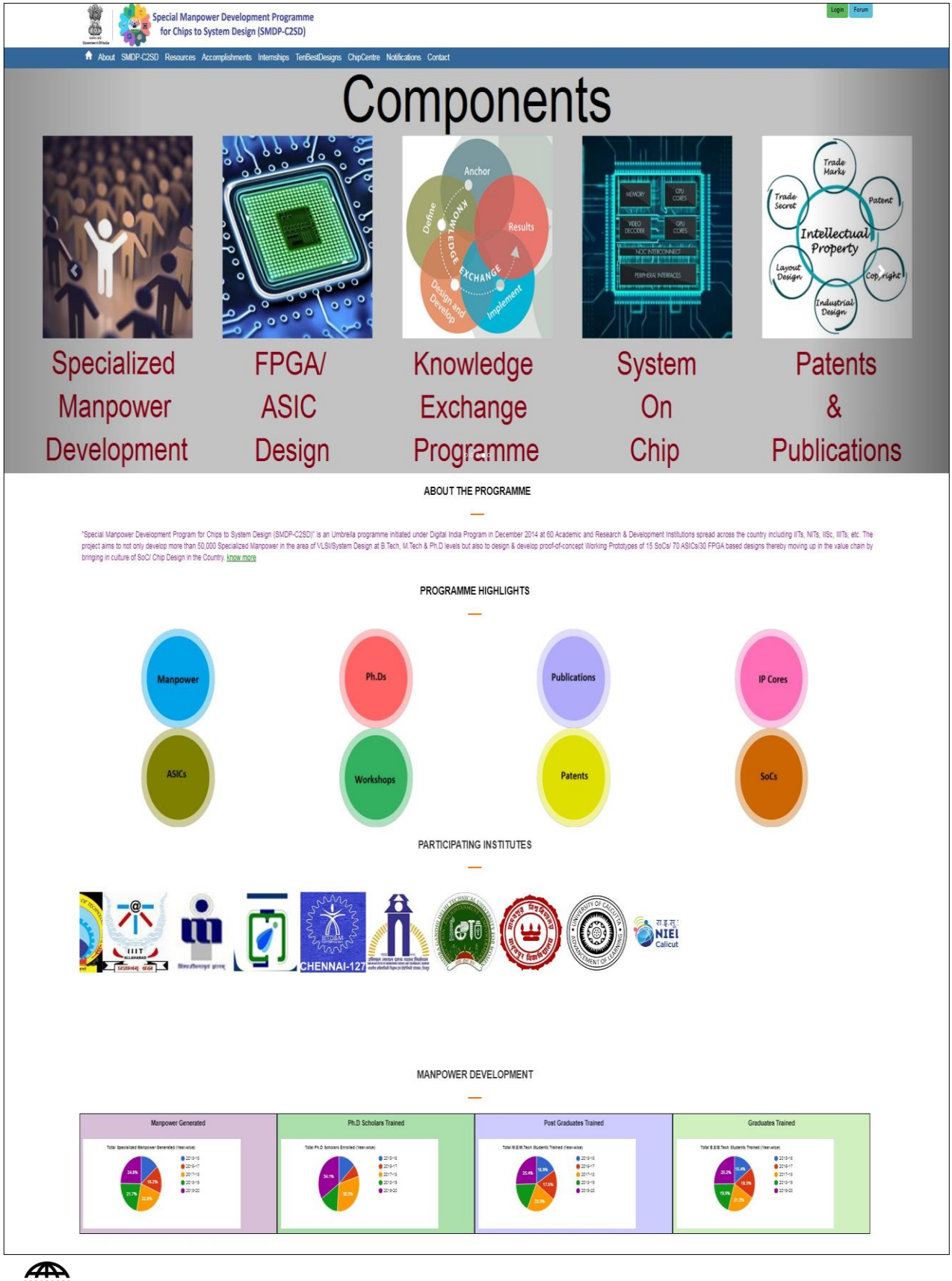
1.3.1.12 Website Development and Web based dissemination of Educational Material

Under the programme, SMDP-C2SD website was developed by CDAC Delhi & being used to disseminate information including educational materials generated through IEP, Short-term courses, training programme on EDA tools, Review meeting, Information about Patent registered, Interactive forums to discuss design issues among researchers from 60 PIs.

The SMDP model of MeitY has been a successful model for targeted manpower development in a niche area. The program has successfully inculcated the culture of System-on-Chip/ System Development using mostly in-house designed ASICs / ICs at Academic institutions along with generation of expertise.

Enhancing the quality of the faculty through IEPs, Workshops etc. would have a long term positive impact on generation of quality manpower in the high technology VLSI Design and System Development

SMDP-C2SD Website http://smdpc2sd.gov.in



2.0 Impact Assessment Report on Special Manpower development Programme for Chips to System Design

Third-party review and evaluation of the SMDP-C2SD Program was conducted by **VLSI Society of India**. For review of Programme activities, several interactions were held between VLSI Society of India, IESA, Participating Institutions and MeitY. Various Programme activity of Programme were analysed and reviewed based on the information available at SMDP-C2SD website http://smdpc2sd.gov.in/.

Based on the objectives and goals of the SMDP-C2SD, assessment across 12 different categories is presented in the following Matrix.

Goal	**Target**	**Achieved**	**Grade**	**Comments**
Manpower Development	50000	100%	A	Quality of the students could be better. Higher % of students in Type-I and Type-II should be targeted.
VLSI Design Laboratories	60	100%	A	Remote & Cloud based access to the infrastructure for Ease of access and better utilization of resources
Development of working prototype systems	15	15	B	Technical content and Commercialization potential could be improved by increasing effective industry participation.
ASIC and Board Level Designs Using FPGAs	30	Goals Achieved	B	Tape-Outs could have better and diverse technical &research contents to cater to wider range of applications
Establishment of Chip Center		Goals Achieved	B+	Turn-around time for Tape-Outs was long and should be improved.
India Chip Program		Goals Achieved	B+	More Tape-Outs at Advanced Nodes as per need of the application.
Instruction Enhancement Program (Faculty Training)	15	Goals Achieved	B	Need more work; Trained and capable faculty is the key to success
International Conference Support		Goals Achieved	B	Bring and Support More International Conference in India. Increase student and faculty participation in international conferences abroad.
Patents and Publications (National, International)		Goals Achieved	A	H-Index and Citation Index need significant improvement.
M. Tech & B. Tech Model Syllabus		Goals Achieved	B	Need AICTE approved B.Tech Program in Electronics & VLSI
Industry and Experts Involvement		Goals Achieved	B	Quality and Quantity of Industry and Global Experts needs improvement
Website Development		Goals Achieved	A	Good Start, Let's device a way to collate all knowledge generated in a systematic manner.
Overall Score			**8.83/10**	

VLSI Society of India has made the following recommendations in respect of future roadmap to broaden & strengthen the base of VLSI design in the country:

(i) **Broaden & strengthen the base of VLSI/ Chip design in the country** by way of including new/ more institutions in next phase of SMDP.

(ii) **Optimal utilization of design infrastructure** to be made in next phase of SMDP by way of making efforts towards cloud based access of EDA Tool license and Compute/ storage infrastructure.

(iii) **Streamlined process for design tape out at foreign foundries** to be worked out by working out advance agreements with demand aggregators (viz. IMEC, Euro practise, e-FAB etc), packaging & board design service providers. Provide opportunities for SMDP-C2SD students/ researchers to undergo research internship at leading fabs.

(iv) **Focus on faculty development by way of implementing collaborating programmes with industry** wherein faculty to spend working at industry and vice-versa. International conferences of repute may be activity supported / organized under SMDP-C2SD.

(v) **Focus on generating Industry-ready manpower** by way of initiating new bachelor's programme in Electronics and VLSI design, providing internship opportunities to students/ researchers.

(vi) **More number of Academia-industry collaborative projects to be supported** for translation of technology by way of regular reviews and identifying/ supporting projects having commercialization potential / part-funding from industry (preferably).

(vii) **Translation of technology** to be encouraged by way of supporting projects focusing on national priorities, part-funding (preferably) from industry and creating linkages with other schemes (i.e. proposed F-DLI (Fabless design linked incentive) Scheme, NIDHI/PRAYAS programme and TBI etc).

The detailed Assessment report is placed at **Annexure A**

3.0 Evolving of Chips to Startup Programme

India's share in the global hardware electronics production is about 3% and the share of domestic electronics production in India's GDP is 2.3%. In 2017-18, the import of electronic goods was of the order of USD 53 billion (approximately INR 3, 44,500 crore) which is expected to rise rapidly to about USD 400 billion (approximately INR 26, 00,000 crore) by 2025 *(Source: NPE 2019)*. With an aim to reduce the import of electronics product and to promote the domestic manufacturing and export in the entire value-chain of ESDM, National Policy on Electronics (NPE)-2019 was formulated to drive the capabilities in the Country by developing core components, including chipsets, core and peripheral IPs, creating an enabling environment for the Industry to compete globally and to Provide support for significantly enhancing the availability of skilled manpower in the ESDM sector.

To fulfil the vision and mission of NPE-2019, there is a fundamental need to create highly skilled and trained manpower in the areas of hardware IPs design, IC design, SoC design, System design and applications. The proposed **"Chips to Startup (C2S)"** Programme addresses each entity of the value chain in Electronics System Design viz. quality manpower training, research and development, hardware IPs design, System design, application-oriented R&D, Prototype design and deployment with the help of Academia, Industry, Start-ups and R&D establishments.

Stakeholder's Consultation: The contours of the proposed C2S Programme has been evolved by following an extensive stakeholder consultation process (involving a number of brainstorming sessions with experts from 60 SMDP-C2SD Participating Institutions, Government organizations, Industry and Industry Association). TAC (Technical Advisory Committee) under the Chairmanship of Prof. Dinesh Kumar Sharma, IIT Bombay while reviewing the progress of present phase of SMDP (viz. SMDP-C2SD) in its 6th meeting, also provided guidance on firming-up the proposal on next phase of SMDP (viz. C2S).

Recommendation by NSC (National Steering Committee): Based on the details presented to NSC in its 5th meeting, NSC under the Chairmanship of Secretary, MeitY, in-principally agreed for initiation of next phase of SMDP (viz. C2S) simultaneously with SMDP-C2SD programme.

Impact Assessment by VLSI Society of India: VLSI Society of India, while carrying out impact assessment of SMDP-C2SD Programme, not only noted its successful implementation but also recommended that the next Phase of SMDP should aim to broaden the VLSI design base by including more number of institutions and facilitate industry-led R&D by way of implementing more collaborative projects with industry targeting import substitution and commercialization. Efforts should be made to make available the facilities provided by the Chip Centre (including the design infrastructure support) in centralized manner, accessible to participating institutions across the country.

Recommendation by Expert Committee: MeitY constituted the Expert Committee under the chairmanship of Prof. Kamakoti, IIT Madras for formulating the future roadmap to broaden & strengthen the base of VLSI design in the country. Expert Committee appreciate the contours of the C2S Programme proposal and recommended its initiation.

4.0 Chips to Startup (C2S) Programme

Ministry of Electronics and Information Technology has come out with National Policy on Electronics 2019 (NPE-2019) with a vision to position India as a global hub for Electronics System Design and Manufacturing (ESDM) by encouraging and driving capabilities in the country for developing core components, including chipsets, and creating an enabling environment for the Industry to compete globally. One of the objectives of National Policy of Electronics is to promote domestic manufacturing including core components and materials and to reduce dependence on import of electronic goods by focusing on skill, technology, scale and the global market with a target to achieve the turnover of USD 400 billion (approximately INR 26,00,000 crore) by 2025.To achieve this target, some of the strategies identified in NPE 2019 are to (i) encourage participation of academic institutes in smaller cities in addition to premier institutes, (ii) bring collaborative R&D between academia and industry iii) Provide support to start-ups in emerging areas/ technologies from supporting the concept to development/ prototyping of products, including the complete value chain (iv) Set up a framework for creation of an ecosystem for promoting design of IPs in the country.

Thus, the National Policy of Electronics not only aims to provide support for significantly enhancing the availability of skilled manpower to the industry but also to encourage the industry led R&D and innovation in all sub-sectors of electronics by promoting path-breaking research, grass root level innovations and early-stage Start-ups in emerging technology Projects.

In line with the objective and vision of NPE-2019, an umbrella programme **"Chips to Startup (C2S)" Programme** has been proposed which not only aims at developing Specialized Manpower in VLSI/Embedded System Design domain but also addresses each entity of the Electronics value chain via Specialized Manpower training, Creation of reusable IPs repository, Design of application-oriented Systems/ASICs/FPGAs and deployment by academia/ R&D organization by way of leveraging the expertise available at Start-ups/MSMEs.

4.1 Objectives

The main objectives of the Chips to Startup Programme (C2S) are:

i. Generating Industry-ready manpower in System/ SoC Design area for creating vibrant fabless chip design ecosystem in the country.

ii. Promoting industry-led R&D, translational research and strengthening Industry-Academia collaboration.

iii. Leapfrogging in ESDM space by way of inculcating the culture of developing reusable IP Cores & developing ASIC/ SoC/ Systems for societal/ strategic sectors.

iv. Broaden the base of ASIC / IC design in the Country by accommodating more academic institutions, start-ups for design of IPs / ASICs / Systems/ SoCs.

v. Protection of Intellectual Property generated etc.

vi. To inculcate the culture of entrepreneurship among students & researchers by way of incubating startups.

4.2 Participating Institutions

The programme would be implemented at about **100** academic institutions/R&D organizations across the Country. Besides them, Start-ups and MSMEs can also participate in the programme by submitting their proposals under Academia- Industry Collaborative Project, Grand Challenge/ /Hackathons/RFP for development of System/SoC/IP Core(s).

4.3 R&D Projects Deliverables and Outcomes

4.3.1 Design and Development of application oriented PoC/Working Prototype/Systems

Under the Programme, based on the Institutions expertise, Technology Readiness Level (TRL) and design experience acquired during earlier SMDP Programmes, it is proposed to invite call for proposal in three different categories from the Institutions, Start-ups and MSMEs for development of frugal solutions in areas like Healthcare/Agriculture/Energy-Environment/Intelligent Transport/Emerging Technology/Safety & Security etc. The purpose of this categorization is to raise the level of technical expertise available at the Institutions by way of developing Proof of Concept (PoC)/Working Prototype/Systems and to facilitate Start-ups/MSMEs for development of Indigenous IP Core/Systems/SoC(s) in collaboration with Academia/R&D Organizations.

A. Category-I: Design and Development of Systems/SoCs/ASICs/Reusable IP Core(s):

Category-I is open to all Academia, Start-up and MSMEs having prior experience on development of Proof of Concept or Working Prototype. Under this category, following three types of projects are proposed to be supported:

i. Academia-Industry Collaborative Projects

To strengthen the Industry interactions with Academia and R&D organizations through collaborative research projects, it is proposed to initiate at least 10 Application-oriented R&D projects jointly implemented by Academia/R&D organizations and Start-up(s)/MSMEs in collaboration with part funding from End user organizations (preferably 10% (or more) of the overall budget as cash and not as kind).

Project proposal, which have already reached up to TRL 7 would be given preference in selection for translation of technology developed by them.

ii. Grand Challenges/Hackathons

To foster the Indian Innovation and Research in the Country by developing affordable and sustainable solutions for Societal Problem catering to both global and domestic requirements, no of Grand Challenges/Hackathons would be organized for Academia/R&D organizations/Start-ups/MSMEs under the Programme.

The winning start-ups of Grand Challenge may also submit project proposal for product development as academia-Industry collaborative project.

iii. RFP for design & development of IP Core(s)/System/SoC design(s)

In order to create an eco-system for globally competitive Indigenous Product and to boost domestic manufacturing in the Country, it is proposed to invite proposal from Academia/R&D organizations/Start-ups/MSMEs in RFP mode for development of IP Core(s)/System/SoC design(s).

B. Category-II: Development of Application Oriented Working Prototype of IPs/ASICs/SoCs

Under this Category, the application-oriented R&D proposals with well-defined specifications for the ASICs/ IPs/ SoCs/System would be invited from the Institution (~40) in Consortium mode. These proposals should have the letter of interest/commitment from end user organization.

C. Category-III Proof of Concept oriented Research and Development of ASICs/FPGAs

To broaden the research base across the country in VLSI/Embedded design area by inclusion of new academic institutions including SC/ST/Minority/Woman institutions, it is proposed to invite R&D Proposal from the (~50) Institutions individually (mostly new) for development of Proof of Concept (PoC) by taking ASIC and FPGA based designs. The proposals having letter of interest from user organizations would be given preference for financial support by MeitY.

4.3.2 Specialized and Trained Manpower Development at B.Tech/M.Tech/PhD level

Under the Programme, it is proposed to include about 100 Institutions (including IITs/NITs/IIITs/Government/Private Institutions) spread across the country based on their interest and expertise in VLSI and Embedded System Design area.

The students at these 100 Institutions would be trained in all aspects of VLSI/Embedded System design by providing exposure of complete Design Cycle including Specification Finalization, Frontend, Backend, GDSII Tape out, Fabrication and Testing. It is proposed to generate 85,000 Specialized Manpower at B.Tech/M.Tech/PhD level as part of the Program. This will include:

- Type-I Manpower (PhD) -200 No.
- Type-II Manpower (M. Tech in VLSI / Embedded System Design) - 7000 No.
- Type-III Manpower (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.) - 8800 No.
- Type IV Manpower (B. Tech with at least two VLSI Courses / minor project in VLSI) - 69,000 No.

Additionally, due to involvement of Industry/Start up in the problem identification and Project implementation, students would also be exposed to the work culture of the Industry/Start-ups which would help them in future for taking such type of project activity.

4.3.3 Access of centralize Electronic Design Automation (EDA) tools facility.

Under the Programme, access of EDA tools facility would be provided to all Participating Institutions in centralize manner for designing of FPGAs/ASICs/SoCs/IP Core(s). This approach would enable the optimal utilization of licenses required by Institutions for development of their designs. It will also cater the requirement of EDA tool of the new Institutions who were not the part of Programme in the beginning.

In addition, training on chip design methodology using EDA tools would also be imparted to the Institutions who are new to chip development activity through NIELIT by way of conducting IEPs/training programmes in coordination with Chip Centre.

4.3.4 Initiation of M.Tech Programme in VLSI/Embedded System design

Efforts would also be made for initiation of M.Tech Program in VLSI/Embedded System at the new Participating Institutions (who do not offer M.Tech course at present) in the first 2-3 years of the program with approval of their competent authorities.

4.3.5 Instruction Enhancement Programmes (IEPs)

The IEPs would be organised by NIELIT Calicut in Emerging Technology area as well as VLSI/Embedded System design which would enable the Participating Institutions to design, develop, and deploy SoCs /ASICs/ Reusable IP cores with targeted applications. Depending on the technical requirements, Industry experts and Experts from EDA tool vendors etc. would also be invited for providing technical sessions as part of the IEPs. 3-4 IEPs per year, totalling 15-20 IEPs, would be organised under the program in Virtual/Physical mode to train the faculty as well as student of Institutions. Recorded technical sessions of the IEPs would also be made available at C2S website.

4.3.6 Online Hardware Training Programme by establishing SMART Remote Lab facility

For proliferation of advanced VLSI and Embedded system design training, research and electronics systems development across the country, it is proposed to set up a Skilled

Manpower Advanced Research and Training (SMART) facility as a remote lab at NIELIT Calicut. The 'SMART' remote lab facility will be available 24x7 and the students, researchers, start-up industries can access the facility, anytime and anywhere.

The remote VLSI and Embedded System design and training facility proposed to be setup at NIELIT Calicut is also targeted to facilitate electronics hardware design technology and training needs for small scale electronics industries, researchers and students across the country. To learn electronics hardware and embedded system concepts, and to acquire the design skills it is inevitable to practice laboratory experiments. The proposed facility will enable generation of skilled manpower as well as, Intellectual Property generation in VLSI, electronics hardware and embedded system design areas. The proposed facility will also enable the remote electronics hardware bring up by enabling the EDA Tools, test & measuring equipment like logic analyzers, spectrum analyzers, digital storage oscilloscope, etc. The facility enables remote hardware debugging like remote medical diagnosis as well.

The objectives of setting up a SMART Remote lab as part of C2S are as follows:

i. A unique national facility for Remote VLSI and Embedded System advanced training.
ii. Setting up of two labs having 100 remote hardware systems each , to train approx. 20,000 Candidates/Year remotely in Electronics hardware design including VLSI Design, Embedded hardware design, board design, etc.
iii. To enable reconfigurable hardware and flexible systems for remote access.
iv. To promote electronics system design across the country, by enabling remote hardware and EDA tool access to small and medium scale industries, researchers and students across the country.
v. To enable remote hardware access to approximately 20,000 Candidates/Year.
vi. Facilitate academic research projects and internships.
vii. Handholding of Startup.

The outreach via of on-line training programs by make using this facility is as follows:

i. Promotion of on-line education in VLSI, embedded systems, and electronics hardware design and technology.
ii. Generation of skilled manpower in electronics hardware and embedded system designs.
iii. Remote debugging of electronics hardware systems like remote medical diagnosis.
iv. Remote board bring up and handholding to startups.
v. Remote application development.
vi. Enable Remote hardware trainings to BIMSTEC countries/Globally.
vii. Remote hardware design access facility to start ups and young researchers.
viii. Resource sharing and infrastructure utilization.
ix. Quality trainings services to masses at affordable cost.

The outcomes of the SMART Remote lab facility are as follows:

i. A remote hardware design and training facility at NIELIT Calicut.

ii. Highly skilled manpower capable of electronics hardware design, embedded system design and electronic product design shall be generated.

iii. Availability of high-end flexible and reusable hardware systems for remote access.

iv. Remote hardware design and debugging laboratory-A national facility.

v. Remote embedded application development facility.

vi. Remote hardware design facility for startups.

vii. Handholding of at least 10 startups for Electronics System Design and Development.

viii. Train around 1 lakh candidates over a period of five years in Electronics Hardware/Embedded System Design and allied areas.

In addition to the conduction of on-line IEPs, the following are the NSQF aligned training programs proposed to be conducted by utilizing this facility.

Sl. No	NSQF aligned Course Name	Duration	Equivalent Academic Credit
1.	Electronic Hardware Design Flow	45 Hours (15 Hours Theory + 30 Hours Practical)	2
2.	Electronic Board Bring Up	45 Hours (15 Hours Theory + 30 Hours Practical)	2
3.	FPGA (Reconfigurable hardware) based Embedded System Design	90 Hours (30 Hours Theory + 60 Hours Practical)	4
4.	Electronic System Design	90 Hours (30 Hours Theory + 60 Hours Practical)	4
5.	PCB Design and Fabrication	45 Hours (15 Hours Theory + 30 Hours Practical)	2
6.	VLSI Design Flow Covering Analog and Digital Design Flow	90 Hours (30 Hours Theory + 60 Hours Practical)	4
7.	VLSI Physical Design	90 Hours (30 Hours Theory + 60 Hours Practical)	4
8.	On-line workshops in VLSI/Embedded /Electronic Product Design.	1-5 days	-
9.	Online Internship Programs VLSI/ Embedded/Electronic Product Design.	1-4 weeks	-
10.	Academic Projects VLSI/Embedded /Electronic Product Design.	6-8 Months	-

4.3.7 Organizing Workshops/Symposiums/Conferences/Webinars

Under the programme, annual Conference/Workshop/Symposium etc. focusing on emerging areas / trends in Microelectronics / VLSI /Embedded System design/Hardware Security would be organized. Leading National / International Experts/guest faculty from Academia/R&D organizations/Industry would be invited to deliver lectures in these workshops /symposiums/webinars. Students/Researchers would also be supported to attend and present the paper in International Conferences for the work carried out under the projects.

ZoPP Workshop

Under the Programme, ZoPP Workshop is proposed to be organised in which the Chief Investigators / Co-Investigators and other collaborators viz. Start-up(s) / End-users / MSMEs would participate and make a detailed presentation on the various works being carried out. Such event would, thus, provide an opportunity to all for getting insight into the various activities being carried out under the programme.

4.3.8 Website Development and dissemination of Educational and Training material

Under the Program, on need basis and on the identified contemporary topics, Specialized Lab Sessions, Educational / Training Material etc. would be developed and disseminated through interactive C2S Website for use of faculty / research scholars / project staffs and students. The Website would also host the recorded IEPs, EDA tools training programme, technical/official interactions between stakeholders, Outcomes etc.

Access of C2S Website would also be provided to all Institutions for hosting the material developed by them.

4.3.9 Setting up the IP Core Repository

A Repository of designs carried out by the participating Institutions under the program would be set up at the Chip Centre. For ready references of these designs, an 'on-line' data-base of the designs available in the Repository would also be developed and made available by Chip Centre at the Website of the program.

4.3.10 India Chip Programme

Under India Chip programme, ASICs designed by the students/researchers of Academia/R&D Institutions/Start-up/MSMEs participating under C2S Programme would be supported for fabrication at Overseas foundry on need basis in Multi Project Wafer (MPW) mode.

The design would be selected for fabrication at overseas foundry or Indian foundry based on their project submission in different project categories. It is proposed to support 4-20 tape out per year at overseas foundry and 2 runs at SCL, however actual fabrication runs required will depend on designs submitted by Institutions to Chip Centre.

4.3.11 Upgradation of Chip Centre

Under Special Development Programme for Chips to System design (SMDP-C2SD), Chip Centre was established at C-DAC, Bangalore for undertaking Siliconization of ASICs/Integrated Circuits designed by the Participating Institution. Chip Centre was the nodal centre for integrating the designs received from institutions and sending them to SCL for fabrication in MPW mode. Chip Centre also facilitated the Institutions in packaging of bare dies received from SCL.

In the present C2S programme, it is proposed that Chip Centre would not only provide fabrication support to all implementing institutions at SCL and overseas foundries (TSMC, UMC, Tower Jazz Semiconductor etc. and through foundry technology channel associates viz. Europractice (IMEC), MUSE, MOSIS) in MPW mode but also offer design services including maintaining IP Core Repository, Fab compliance validation of designs, design flow establishment with a specific set of EDA tools and the Fab PDK, Packaging of Chips, Testing, Characterization in the Country in centralized manner.

4.3.12 Establishment of Design Centre

To streamline the adoption of a standardized VLSI design flow process among Academia and Start-ups and for timely completion of design and development, a Design Centre would be setup at CDAC Bangalore as a part of Chip Centre.

The Design Centre would be a nodal centre in the Country who will be handholding the new Institutions/Start-up participating under the Programme for their ASIC and FPGA based designs.

4.3.13 Development of Model Syllabus and adoption by Academia

With a view to promote VLSI/Embedded System design in the country, a model syllabus for B.Tech / M.Tech oriented towards SoC / System Designing will be prepared. This model curriculum would be a structured curriculum which will include practical work / minor projects etc. The faculty of academia and other experts including experts from the industry would be involved to work out the Model Syllabus. Efforts would be made for adopt the model syllabus in their course curriculum within two years of initiation of the programme with the approval of their competent authorities.

4.3.14 Protection of Intellectual Property (IPs) Core Generated

Intellectual Property (IP) generated in a technology programme is one of its most valuable assets. Thus, protecting intellectual property developed is crucial to the success of programme.

To protect the IP generated, Institution would be encouraged to file Patents, Protection of ASICs/IP Core (under Semiconductor Integrated Circuits Layout-Design Circuits Layout-Design Act) etc. developed under the Projects. It is expected that about 30 IP Core(s) may be generated during the course of the Program. Fund Provision would be kept for filing of Patents of the IP Core(s) generated.

4.3.15 Patents/Publications

The faculty / students / researchers of the Institutions participating in the programme would be encouraged to publish the papers in journals/ present papers in conferences and to file patents based on their original research work carried out by them as part of the program. The financial support would be provided to authors whose papers are selected in conferences of repute say IEEE conference etc. It is expected that around 2000 publications and 50 patents would be filed for the research work carried out under the Projects.

4.3.15 Enrolment of PhDs under Visveswarya PhD Scheme

Under C2S Programme, about 100 Institutions would be responsible for developing working prototypes of 20 System/SoCs, 175 ASICs and 30 FPGA based designs. The project staff to be recruited under the project by 100 Institutions would be involved in VLSI lab and manpower development activity in addition to System/ASIC/FPGA implementation. It is envisaged that the PhD students as Project staff would play a key role in undertaking System/IP development activity at 100 Institutions for the project having duration of 3 to 5 Years.

In view of this, under the programme, it is proposed to keep a provision of enrolment of 200 PhD students (40 PhDs per Academic year (35 Full Time + 5 Part Time) of 100 Institutions under the MeitY supported Visveswarya PhD scheme. Funds for fellowship etc. for these 400 PhDs students would be made available from Visveswarya PhD scheme.

4.3.15 Summary of Outcomes

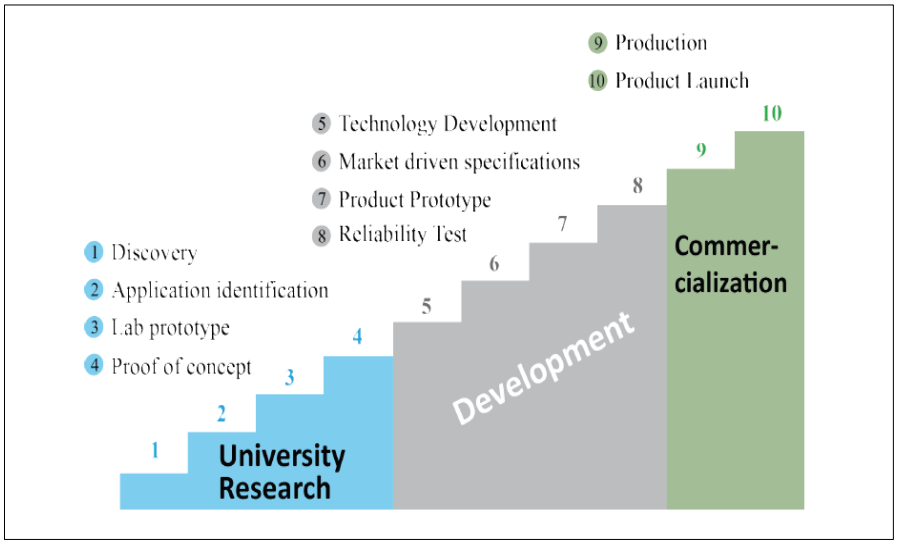
S.No	Project Activities	Outcomes	
1.	Development of Systems/ SOCs /ASICs/ FPGA Based designs	**System/SoCs** : 20 **ASIC** : 175 **FPGA Based Designs** : 30	
2.	Manpower	Total 85,000	
		Type-I Manpower (PhD)	200
		Type-II Manpower (M. Tech in VLSI / Embedded System Design)	7000
		Type-III Manpower (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.)	8800
		Type IV Manpower (B. Tech with at least two VLSI Courses / minor project in VLSI)	69000
3.	Setting up the Reusable IP Core Repository	Repository of 30 No. reusable IP Cores would be created	
4.	Patents/Publications	50 Patents/ 2000 Publications in Journals and Conferences	
5.	Start-ups Incubation	25 Start-ups would be incubated from the Institutions	
6.	Transfer of Technologies	At least 10 Technologies would be transferred to Industry/R&D Organizations for Commercialization	
7.	Instruction Enhancement Program (IEP)	20 Instruction Enhancement Program in various topics would be conducted for knowledge enhancement of Faculty, Project Staff and Students of Participating Institution.	
8.	Online Hardware Training Programme through SMART Remote Lab facility	A SMART Remote lab facility would be set up for hand holing of at least 10 Start-ups and to train around 1 lakh Candidates over a period of five years in Electronics Hardware/Embedded System Design and allied areas	
9.	Initiation of M.Tech Programme	Initiation of M.Tech Programme at the new Participating Institutions (who do not offer M.Tech course at present) in the first 2-3 years of the program	
10.	Enrolment of PhDs under Visvesvaraya PhD scheme	200 PhDs students (40 PhDs per Academic year (35 Full Time + 5 Part Time) of 100 Institutions would be supported under Visvesvaraya PhD scheme of MeitY	
11.	Web based dissemination	All educational materials developed under the program would be disseminated through the **C2S** Website.	
12.	Fabrication support to 100 Institutions/Start-up/MSME	Fabrication support for design developed by SMDP Institutions/Start-ups/MSMEs would be provided at SCL and Overseas Foundry under India Chip Programme	
13.	Workshop/ Symposium/ Conferences/Webinars	Conference/Workshop/Symposium/Webinars etc. would be organized focusing on emerging areas / trends in Microelectronics / VLSI /Embedded System design/Hardware Security.	
14.	Upgradation of Chip Centre and establishment of Design Centre	For undertaking siliconization of chips a dedicated centre having capability to integrate MPW would be set up to service all ASIC prototyping and fabrication including testing.	

5.0 Categories of Projects Funding - Criterion, Classification and Outcomes

Under the Programme, based on the Institutions expertise, outcome in terms of SoCs/ASICs/FPGAs acquired during earlier SMDP Programmes and Technology Readiness Level (TRL), Projects have been categorized in three different Categories. The details of TRL criteria and Project Categories are given below:

5.1 Criteria for Monitoring Technology Readiness Level (TRL)

The maturity of technology is measured by Technology Readiness Levels (TRL). It is generally measured in the scale from 1 to 9. A project is evaluated against set parameters for each TRL and is rated based on its progress.



TRL	Stage	Definition	Exit Criteria to achieve the given TRL
1.	**Discovery**	**Review of Scientific Knowledge Base** **(i) Scope**: Fundamental research begins, postulating basic principles having no experimental proof, which can be translated into applied R&D. This may include: a. Surveying published research of a technology's basic properties. b. Identifying essential characteristics & behaviours of systems & architectures using mathematical formulations or algorithms. **(ii) Activities**: a. State the challenges that the industry or other users face and the need for a new kind of innovation such as variety, practice, or other technology solution. b. Estimate the value of the innovative solution compared to the existing variety, practice, or other technologies, and where the solution fits in the overall supply chain.	Peer reviewed publication of research underlying the proposed concept/application. (i) Do basic scientific principles support the concept? (ii) Has the technology development methodology or approach been developed?
2.	**Application identification**	**Technology concept formulation and application identification.**	Documented description of the application/concept that addresses

		(i) **Scope**: Applied research on how technology could be applied in the market. Potential of the prospective system applications is speculative and inferred from general assumptions or some analytical data obtained from publications or other references. (ii) **Activities**: a. Based on the competitor analysis & patent landscaping, characteristics of the applications are described (future viability, risks involved and required efforts to advance to next TRL etc.) b. Analytical tools are developed for simulation or analysis of the application.	feasibility and benefit. (i) Are potential system applications identified? (ii) Are system components and the user interface at least partly described? (iii) Do preliminary analyses or experiments confirm that the application might meet the user need?
3.	**Proof-of-Concept**	**Proof-of-concept demonstrated, analytically and/ or experimentally** **(i) Scope:** Active research & development on proof-of-concept development, analytically and/ or experimentally at a lab scale. (ii) **Activities:** Analytical studies and laboratory scale studies to physically validate the analytical predictions of separate elements of the technology (example includes components that are yet not integrated or representatives).	Analytical/experimental proof-of-concept results validating predictions of key parameters. (i) Are system performance metrics established? (ii) Is system feasibility fully established? (iii) Do experiments or modelling and simulation validate performance predictions of system capability? (iv) Does the technology address a need or introduce an innovation?
4.	**Lab Prototype**	**Technology basic validation in a laboratory environment** **(i) Scope:** A low fidelity system/component breadboard is built in close consultation with end-user and operated to demonstrate basic functionality **(ii) Activities:** Estimation using lab-prototype: a. High-level performance and/or operations-oriented metrics. b. Expected operational environments c. financial metrics (cost-benefit analysis) Predictions are defined relative to the final operating environment.	Documented Test performance results using lab prototype demonstrating agreement with analytical predictions and definition of relevant environment. (i) Are end-user requirements documented? (ii) Does a plausible draft integration plan exist, and is component compatibility demonstrated? (iii) Were individual components successfully tested in a laboratory environment (a fully controlled test environment where a limited number of critical functions are tested)
5.	**Technology Development**	**Technology basic validation in a relevant environment.** **Scope:** Testing a high-fidelity Lab-scale system in a simulated/ representative environment. **Activities:** a. The basic technological components are integrated in simulated environment so that the system configuration (at the component-level, sub-system level, and/or system-level) is similar to the final applications in almost all respect. b. Technology assessment could be organized and implemented by either the customer organization, or the technology development organization. c. An assessment to be conducted as part of a critical design review (CDR), or a preliminary design review (PDR) for the system project. Such an assessment effort should also involve where possible those technologists and engineers who were involved in demonstrating the new technology earlier, as well as and independent reviewers representing the management of system project organization.	Documented results of laboratory testing in simulated environment. Identified barriers for target performance goals and plans to overcome them. (i) Are external and internal system interfaces documented? (ii) Are target and minimum operational requirements developed? (iii) Is component integration demonstrated in a laboratory environment (i.e., fully controlled setting)?

6.	**Market Driven Specifications**	Technology model or prototype demonstration in a relevant environment. **Scope**: Testing an engineering-scale fully-functional prototype system in a simulated/ representative environment with full-scale realistic problems. **Activities**: An assessment of technology readiness must involve not only the technologists and engineers involved in demonstrating the new technology and independent reviewers representing the management of their organization, it must also involve technically competent representatives of prospective customers for the new technology. This technology assessment should be organized and implemented by the customer organization, rather than the technology organization.	Documented test performance in simulated lab environment demonstrating agreement with analytical predictions. (i) Is the operational environment (i.e., user community, physical environment, and input data characteristics, as appropriate) fully known? (ii) Was the prototype tested in a realistic and relevant environment outside the laboratory? (iii) Does the prototype satisfy all operational requirements when confronted with realistic problems?
7.	**Product Prototype**	**Technology prototype demonstration in an operational environment.** **Scope**: Demonstration of an actual system prototype in an operational environment (e.g., in the field, on aircraft, in a vehicle, or in space). **Activities**: a. Extensive field trials (Multi-location or hotspots) or other technology performance experiments to be conducted to determine the potential yield, product quality etc. b. Manufacturing lines established or such facility identified.	Documented test performance in operational environment demonstrating agreement with analytical predictions. (i) Are available components representative of production components? (ii) Is the fully integrated prototype demonstrated in an operational environment (i.e., real-world conditions, including the user community)? (iii) Are all interfaces tested individually under stressed and anomalous conditions?
8.	**Reliability Test**	**Actual technology/ System completed and qualified through test and demonstration** **Scope:** Produce certified planting materials or other kinds of technologies and ensure that these can be sourced or are workable for full-scale production. Also, operational efficiency, costs and returns or resource quality improvements that would result from the innovation are established. The system, fully integrated with operational H/w & S/w, is qualified through test and demonstration and Technology has been proven to work in its final form and under expected conditions. **Activities:** a. All functionality tested in simulated and operational scenario. b. Verification & Validation (V&V) and Evaluation completed. c. Commercial manufacturing license obtained, or arrangement done in this regard.	Documented Results of testing in its final configuration. Assessment of it meeting its operational requirements. (i) Are all system components form-, fit-, and function-compatible with each other and with the operational environment? (ii) Is the technology proven in an operational environment (i.e., meet target performance measures)? (iii) Was a rigorous test and evaluation process completed successfully? (iv) Does the technology meet its stated purpose and functionality as designed
9.	**Production**	**Actual technology qualified through successful mission operations or in market.** **Scope:** Commercial-scale production by producers or manufacturers occurs with delivery of products to producers, handlers, processors, distributors, or other supply chain participants to market outlets and for meeting user demand. **Activities:** a. Commercialization initiated and sustaining engineering support in place. b. All documentation completed.	Report on performance of actual operation of the product / technology in its final form, under the full range of operating conditions. (i) Is the technology deployed in its intended operational environment? (ii) Is information about the technology disseminated to the user community? (iii) Is the technology adopted by the user community?

5.2 Project Categorization

With a focus to develop frugal solutions around societal problem, it is envisioned that, under the programme, the project would be initiated in following key areas:

- Energy & Environment
- Healthcare
- Agriculture
- Disaster Management
- Intelligent Transport System
- Emerging Technology
- Safety & Security
- Strategic Sector etc.

R&D proposals in these areas would be invited from the Institutions under 3 different project categories. The purpose of this categorization is to raise the level of technical expertise available at the Institutions by way of developing Proof of Concept (PoC), Working Prototype and to facilitate Start-ups/MSMEs for taking this forward to commercialization. The details of project category are given below:

5.2.1 Category-I: Design and Development of deployable Systems/SoCs/ASICs/Reusable IP Cores

Category-I is open to all Academia/R&D Organizations who have the prior experience on development of at least Proof of Concept or Working prototype and for Indian Start-ups & MSMEs. Under this category, following three types of project activity are proposed to be supported:

A. Academia-Industry Collaborative Projects

To strengthen the industry interactions with Academia and R&D organizations through collaborative research projects, it is proposed to initiate at least 10 application-oriented R&D proposals jointly implemented by Academia/R&D organizations and Indian Start-up(s)/MSMEs with part funding from End User Organization (preferably 10% (or more) of the overall budget as cash and not as kind).

Project proposals, which have already reached up to TRL 7 would be given preference in selection for translation of technology developed by them.

The duration of such proposals would be up to 3 years with targeted Technology Readiness Level (TRL)-7 and above. The proposal would be supported for fabrication at overseas foundry/SCL depending on the needs of the project.

Milestones linked Grant-in-Aid (GIA) support would be provided to Academia, R&D Organizations, Start-up and MSMEs for Project implementations.

Note: Institutions applying under this category may individually submit Research Project proposal in Emerging areas. Such proposal would only be supported for design Infrastructure support.

B. Grand Challenges/Hackathons

To foster the Indian Innovation and Research in the Country by developing affordable and sustainable solutions for Societal Problem catering to both global and domestic requirements, no of Grand Challenges/Hackathons would be organized for Academia/R&D organizations/Start-ups/MSMEs under the Programme.

The winning start-ups of Grand Challenge may also submit project proposal for product development as academia-Industry collaborative project.

C. RFP for design & development of IP Core/System/SoC(s)

In order to create an eco-system for globally competitive Indigenous Product and to boost domestic manufacturing in the Country, it is proposed to invite proposal from Academia/R&D organizations/Start-ups/MSMEs in RFP mode for development of IP Core(s)/System/SoC design(s).

5.2.2 Category-II: Development of Application Oriented Working Prototype of IP Core(s)/ASICs/SoCs

Under this Category, the application-oriented R&D proposals (with duration up to 5 Years and targeted TRL level up to 7) would be invited from the Institution (~40) in Consortium mode for development of ASIC/ SoC/System/IP Core(s). Such proposals should have the letter of interest/commitment from end user organization.

Any Institution other than 10 Resource Centre of SMDP-C2SD Programme (including IIT Kharagpur, IIT Bombay, IIT Madras, IIT Kanpur, IIT Delhi, IIT Guwahati, IIT Roorkee, IISc Bangalore, CEERI, Pilani, VNIT, Nagpur) can submit their proposal in Cluster of maximum 5 Institutions. Therefore, minimum 10 working prototypes of silicon proven IPs / ASICs / SoCs/Systems are expected to be delivered by 40 Institutions under this category. These proposals would be supported for fabrication at overseas foundry/SCL depending on the needs of the project.

Note: Institutions applying under this category Projects may individually submit Research Project proposal in Emerging areas. Such proposal would only be supported for design Infrastructure support.

5.2.3 Category-III Proof of Concept oriented Research and Development of ASICs/FPGAs

To broaden the research base across the country in VLSI/Embedded design area by inclusion of new academic institution including SC/ST/Minority/Women institutions, it is proposed to invite call for Proposal from the (~50) Government Institutions (mostly new) for development of Proof of Concept by taking ASIC and FPGA based designs with duration of 5 years and targeted Technology Readiness Level up to 4. The proposals having letter of interest from end user organizations would be preferred for financial support by MeitY.

Under this Category, proposals for development of ASIC and FPGA based designs would be invited from Government Institutions including SMDP-C2SD category III Institution (including NIT Agartala, NIT Patna, NIT Raipur, NIT Sikkim, NIT Goa , NIT Arunachal Pradesh, NIT Meghalaya, NIT Nagaland, NIT Manipur, NIT Mizoram, NIT Uttarakhand, NIT Delhi, NIT Puducherry, IIT Allahabad, ABVIIITM Gwalior, PDPMIIIT(D&M) Jabalpur, IIIT(D&M) Kanchipuram, NIELIT Calicut, University of Calcutta, Indira Gandhi Technical University for Women, Delhi) for duration of 5 year. Such proposal would be supported for fabrication at SCL only.

Like SMDP-C2SD programme, to continue the VLSI design culture at North Eastern region, it is proposed to include 8 North East Institutions (NIT Sikkim, NIT Mizoram, NIT Meghalaya, NIT Agartala, NIT Manipur, NIT Nagaland, NIT Arunachal Pradesh, NIT Silchar) and IIITs under the Programme.

Keeping in view that most of the SMDP-C2SD Category III Institutions were earlier involved in development of FPGA based designs, it is envisaged that these institutions would preferably submit R&D proposals for ASIC based designs.

To encourage the students/researchers from private SC/ST/Minority/Women community towards development in VLSI and Embedded System design area, SC/ST/Minority and Women University/Institution recognized by government would also be made part of the programme.

In summary, Project Categorization is given in table 5.1 below:

Table 5.1: Project Categorization

Institution Category		Institutions/Projects	Project Types	Funds	Industry Support	Fabrication Support
Cat-I*	Open to Academia/R&D Organizations /Indian Start-ups/MSMEs	10 institutions	**A)** Industry- Academia Collaborative Projects (SoC/ System) – **TRL 7 and above (Duration up to 3 years) (project already reached at TRL 7 would be preferred**) **B)** Grand Challenges/ Hackathons /RFP for development of IP Core/System /SoC	Rs. 70 Crore**	Interest from user organization (**preferably 10% (or more) part-funding from End user Organization)**	Prevalant foundry
Cat-II*	Open to Academia/R&D Organizations (Other than Cat-I institutions participated under SMDP-C2SD#)	40 Institutions	**C)** Clustered R&D Project – **target TRL 7 (Duration up to 5 years, Max Cluster Size: 5)**	~ Rs. 80 Crore**	Interest from user organization	Prevalant foundry
Cat-III	Open to Government Academic Institutions (Other than Cat-I/ Cat-II institutions participated under SMDP-C2SD #)	50 Institutions	**D)** Individual ASIC/ FPGA/COTS based development projects for Duration of **5 Years** and TRL **up to 4**		Preferably Interest from user organization	SCL 180nm

***** Institution applying under Category I & II may submit individual research project in emerging areas for duration up to 5 years. Such proposal would only be supported for Infrastructure like EDA tool access and fabrication support in MPW mode.

****** Design infrastructure support (EDA tools, Fabrication, Chip Centre, PCI, Training etc.) worth Rs. 100 Crore in consolidated manner would be made available to all implementing institutions.

List of Category –I & II Institutions participated under SMDP-C2SD Programme is given in table 5.2 below

Table 5.2: List of Category I & II Institutions participated under SMDP-C2SD Programme

Category I	Category II
1. IIT Kharagpur	1. NIT Srinagar
2. IIT Bombay	2. DBRANIT Jalandhar
3. IIT Madras	3. NIT Hamirpur
4. IIT Kanpur	4. NIT Kurukshetra
5. IIT Delhi	5. Thapar University Patiala
6. IIT Guwahati	6. MNIT Jaipur
7. IIT Roorkee	7. MNNIT Allahabad
8. IISc Bangalore	8. IIT(BHU) Varanasi
9. CEERI, Pilani	9. NIT Durgapur
10. VNIT, Nagpur	10. NIT Silchar
	11. IIEST Shibpur
	12. PSG College of Technology, Coimbatore
	13. NIT Jamshedpur
	14. NIT Rourkela
	15. NIT Warangal
	16. NIT Surathkal
	17. SVNIT Surat
	18. MANIT Bhopal
	19. SGSITS Indore
	20. NIT Calicut
	21. NIT Tiruchirappalli
	22. Jadavpur University
	23. IIT Mandi
	24. IIT Ropar
	25. IIT Jodhpur
	26. IIT Bhubaneshwar
	27. IIT Gandhinagar
	28. IIT Indore
	29. IIT Hyderabad
	30. IIT Patna

6.0 Programme Implementation

6.1 Participating Institutions

The programme would be implemented at about 100 Institutions across the Country. Like SMDP-C2SD programme to continue the VLSI design culture at North Eastern Region, it is proposed to include all 8 North East Institutions (NIT Sikkim, NIT Mizoram, NIT Meghalaya, NIT Agartala, NIT Manipur, NIT Nagaland, NIT Arunachal Pradesh, NIT Silchar) under the Programme. To encourage the SC, ST, Minority and Women researchers towards development in VLSI/Embedded System design area, government recognized SC/ST/Minority/Women University/Institutions would also be made part of the Programme.

Besides Academia and R&D Organizations, Start-ups and MSMEs can also participate under the Programme by way of submitting the proposals under Industry Academia collaborative Projects/Grand challenges/RFP.

6.1.1 Eligibility Criteria for Participating Institution

The Academic/R&D Organization who have the pre-existing Lab infrastructure, experienced Faculty in VLSI domain would only be eligible to participate under the Programme.

All Institutions falling in the following categories are proposed to be eligible to participate in the programme and receive funding:

1. Indian Institutes of Technologies (IITs)
2. National Institutes of Technologies (NITs)
3. Indian Institutes of Information Technology (IIITs)
4. Indian Institutes of Science Education and Research (IISERs)
5. Central Universities/Deemed Universities under Central/State Government
7. Colleges/Institutions of National Importance/Eminence
8. R&D Organizations/Institutions (having B.Tech /MTech/PhD courses)
9. Private Universities/ Private Deemed Universities/Private Colleges**

** Private Institutions are also proposed to be eligible for participation in the programme subject to meeting the additional eligibility criteria classified as **Clause (A) and Clause (B)**

Clause (A) Criterion for Institutions which have existing M Tech in VLSI / Micro-electronics or equivalent

- Institutions that have existing post graduate stream in VLSI / Microelectronics / Electronic Systems / Integrated Circuits / ESDM or equivalent and have produced M Tech / PhDs in these areas for the last 3 years. The PhD student(s) are being admitted as per UGC admission norms.

- Institutions should be recognized by AICTE and NBA (National Board of Accreditation) accredited with respect to VLSI / Microelectronics / Electronic System / Integrated Circuits / ESDM or equivalent Programmes.

(OR)

- The Institution should be accredited by NAAC (National Assessment and Accreditation Council of UGC).

Clause (B) Criteria for Institutions which don't have existing M Tech in VLSI / Micro-electronics or equivalent, but to initiate M Tech programme in VLSI / Micro-electronics or equivalent

- Institutions should have existing B.E./B.Tech streams in Electrical/Electronics/ Communication Engineering and have produced M.Tech in other areas for the last 3 years.

- Institutions should be recognized by AICTE and NBA (National Board of Accreditation) accredited for OTHER specializations (other than VLSI / Microelectronics etc.) M Tech programmes.

(OR)

- The Institution should be accredited by NAAC (National Assessment and Accreditation Council of UGC).

All new institutions who were not the part of earlier SMDP programmes would need to furnish copy of documents in support of meeting the above-mentioned eligibility criteria to the Microelectronics Development Division, MeitY for considerations of the submitted proposals under the programme.

The proposals received from the Academic Institutions will be subjected to the scrutiny and evaluation by the Screening Committee and other proposal Review Committees for approval.

6.1.2 Eligibility Criteria for Start-up/MSME

Start-up and MSME participating under the programme are defined as per the extant norms notified by DIPP/Ministry of MSME

6.2 Programme Coordination Institute (PCI)

C2S Programme is expected to cater about 100 Academic/ R&D Institutions spread across the country and Indian Start-ups/MSMEs through collaborative project/Grand Challenges/RFP. For successful implementation of the Programme at 100 Institutions, Project Coordination Institution (PCI) would be setup for regular coordination of technical & financial project activities as well as providing administrative support the Program Division of MeitY. Since during SMDP-C2SD Programme, CDAC Bangalore was associated as Chip Centre and for other programme coordination activity, it is proposed to designate CDAC, Bangalore as PCI under the Programme.

The detailed roles and responsibilities of PCI under C2S are listed below:

i. Centralized Procurement of Proprietary EDA tools, FPGA Boards and other Hardware/Software platforms and provide access to all implementing institutions.

ii. Regular monitoring and reviewing of technical and financial progress of various activities of the program by organizing review committee meetings.

iii. Development of C2S Website and Coordination with web development team of the project for regular updation of data including IEPs, Training Programme, Learning materials, Technical/Official interactions between stakeholders, Project outcomes etc.

iv. Expert Committee formulation for review of Institution's Projects.

v. Organizing Grand Challenges/Hackathons, announcement and execution of RFP.

vi. Provide support for registration to Startups, incubated under the Programme.

vii. Interaction with End Users/Industry for possible Commercialization & Transfer of Technology.

viii. Obtain Memorandum of Understanding from all the Participating Institutions/Startups/MSMEs.

ix. Release of funds to implementing organizations after MeitY approval based on recommendation of review committee.

x. Obtain Fund requirement, Utilization Certificates, Audited statement of Accounts from implementing organizations and release of GIA to them based on the approval of Review Committees.

xi. Regular updation of expenditure details at PFMS EAT 2 module

xii. Coordinating Patenting the R&D work carried out under the programme.

xiii. Coordinating Workshops (ZOPP)/Conferences/Symposium and Paper presentation in International Conferences by students and researchers.

xiv. Coordination with NIELIT Calicut for organizing IEPs and Hardware training Programme.

xv. Preparation of periodic Project Progress Report, maintaining technical and financial database of the project activities supported under the program.

xvi. To track the performance of Institutions for employability of manpower generated, absorbed by Semiconductor design houses, entrepreneurship culture resulted / inculcated.

xvii. Coordinate any other related activity for the smooth implementation of the project and timely completion.

The following is the proposed expenditure for **PCI at CDAC Bangalore** for overall Project Implementation & Coordination:

(Rs. in Lakh)

#	Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
1	Capital Equipment	8.00	4.00	2.00	2.00	2.00	18.00
2	Consumables	2.00	2.00	3.00	2.00	1.00	10.00
3	Manpower	59.00	65.00	71.00	78.00	86.00	359.00
4	Travel & Training	2.00	2.00	1.50	1.50	1.00	8.00
5	Contingencies	2.00	2.00	2.00	2.00	2.00	10.00
6	Overheads, if any	3.00	3.00	3.00	3.00	3.00	15.00
Total		**76.00**	**78.00**	**82.50**	**88.50**	**95.00**	**420.00**

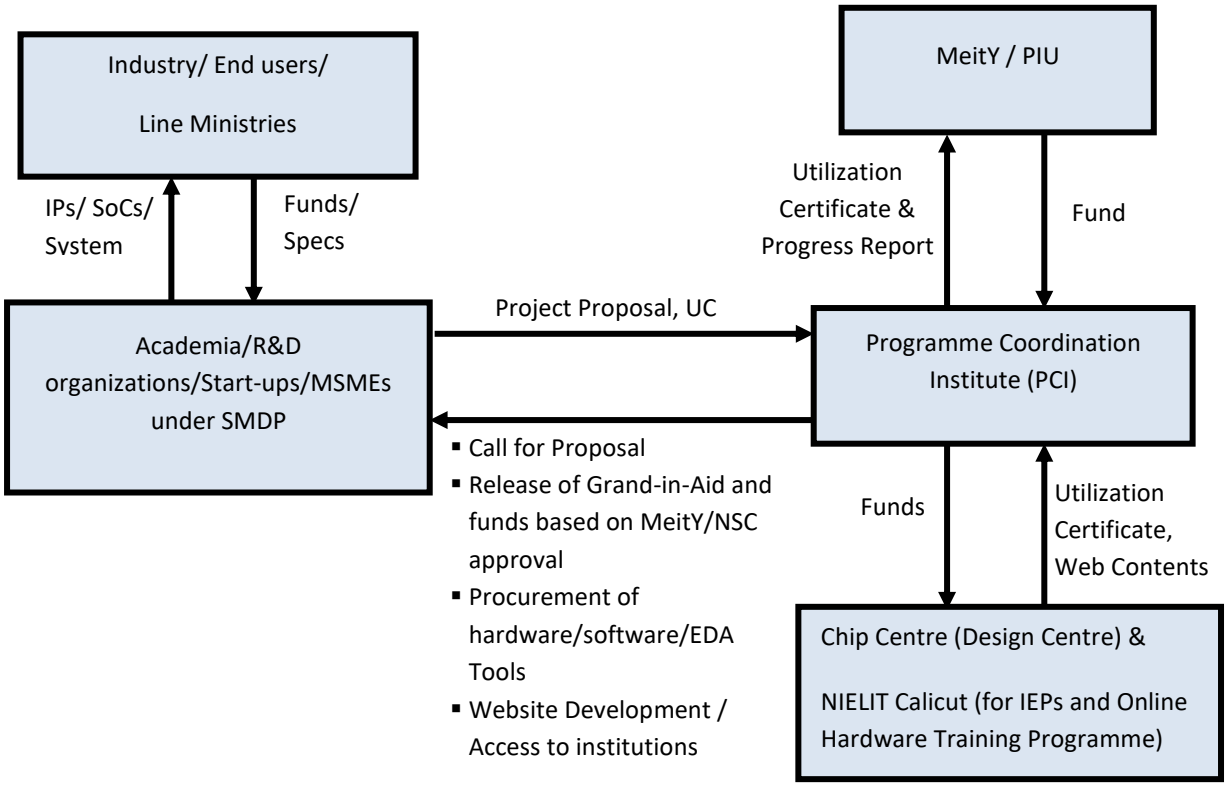


Fig. 6: PCI Operational Mechanism

6.2.1 Project Implementation Unit (PIU)

To provide regular assistance to Program Division of MeitY for monitoring and reviewing of technical & financial activities under the Programme, it is proposed to set up PIU at MeitY as a part of PCI. The following is the proposed expenditure for setting up the PIU at MeitY:

(Rs. In Lakh)

#	Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
1	**Manpower**						
1.1	Senior Consultant (1 No.) (B.E/B.Tech/M.E/M.Tech/PhD) @ Rs. 1.00 lakh per month + 10% increment per annum	12.0	13.2	14.52	15.98	17.58	73.28
1.2	Consultant (MBA/MCA) (1 No.) @ Rs. 0.60 lakh per month + 10% increment per annum	7.2	7.92	8.72	9.6	10.56	44.00
1.3	M.T.S (1 No) @Rs. 0.20 lakh per month + 10% increment per annum	2.4	2.64	2.91	3.20	3.52	14.67
	Total	**21.6**	**23.76**	**26.15**	**28.78**	**31.66**	**131.95**
2	**Infrastructure including H/w, S/w, consumables, contingencies, Travel etc**	3.61	3.61	3.61	3.61	3.61	18.05
	Grand Total	**25.21**	**27.37**	**29.76**	**32.39**	**35.27**	**150.00**

6.2.2 C2S Web Site

For the smooth coordination of the proposed activities and information dissemination, there is a need of development of dedicated interactive Web Site for the Programme. PCI, CDAC Bangalore would be responsible for the development as well as maintenance of Website for entire duration of Programme through an identified agency in consultation with MeitY. A budget of Rs 30.00 Lakh has been earmarked for website development and maintenance activities.

The Website would hold all the requisite information of the Programme including:

i. Online submission of Project Proposal, Evaluation and Monitoring of projects after initiation.

ii. Details of the Projects undertaken in three Project Categories, details of collaboration between Industry and Academia/R&D organizations, IP Core Repository etc. and their latest status.

iii. Announcement of MPW timelines, Grand Challenge, Hackathons and RFP for design and development of IP Core/System/SoC.

iv. Announcement of IEPs/Training Programme/Workshops/Conferences/Symposiums/ Webinars etc.

v. Design submission Section for online submission of designs for fabrication through Chip Centre.

vi. Details of the Systems/SoCs/ASICs/IP Core(s) developed under the Programme.

vii. Details of the manpower generated/Paper/publication/IEP/Training programme/ Workshops/Symposium etc.

viii. Details of the Hardware/Software/FPGA Boards/EDA Tools etc. provided to Institutions/ Start-ups/MSMEs, Chip Centre and Design Centre

ix. Details of Smart lab facility setup by NIELIT Calicut for online Hardware training programme.

x. Dissemination of Educational / Study / Training Materials including the contents created out of IEPs / Symposiums / Conferences etc.

xi. Details of the Chief Investigators (CIs) at Academia, R&D organization, Start-up and MSME.

xii. Development of interactive discussion forum for interaction among researcher, faculty, Chip Centre, Design Centre, Start-ups, MSMEs etc.

xiii. Login Access for (i) CIs of Participating Institutions, (ii) MeitY (iii) PCI (iv) member of review committee (v) Other collaborators

xiv. Other details which are required under the program and deemed fit for display.

6.3 Monitoring and Review Mechanism

The monitoring and reviewing of the Program will be a 3-tier mechanism.

(i) The National Steering Committee,

(ii) Technical and Advisory Committee and

(iii) Project Review and Steering Groups.

All Committees comprising of experts from Line Ministries, Industry, Academia and R&D organizations would provide guidance/suggestions to all implementing institutions for achieving the aims and objectives of the program.

A. National Steering Committee (NSC)

The NSC-an apex body, to be chaired by Secretary, MeitY would be responsible for overall Implementation of the Programme. The other members of the committee will be included from

- Senior officials from Line Ministries/ Government Organizations.
- Experts from Academic institutes
- Experts from Renowned Research laboratories/Organizations
- Officials from User Agencies
- Experts from VLSI Industry/Association.

Terms of Reference of National Steering Committee:

i. Approval of proposals based on recommendation of Evaluation Committee constituted for evaluation of proposals received through Call for Proposal

ii. Evolve and approve the initiation of RFP for development of IP Core/System/SoC, Grand Challenges/Hackathons in line with the aim of the program.

iii. Approval for inclusion of new institutions as Participating Institution and any other new activities as recommended by TAC.

iv. Recommend selection of Institution in particular project Category defined under the Programme for providing support.

v. Regularly review the progress and achievements of the Programme.

vi. Technical and Financial approval, scrutiny & approval for grant-in-aid release from Nodal agency to Participating institutions/Start-ups/MSMEs within the overall approved project outlay.

vii. Approve the redistribution of funds among the different budget heads whenever necessary as per rules of MeitY.

viii. Recommend specific responsibilities to Participating Institutions/Start-ups/MSMEs and the PCI to ensure smooth implementation and progress of the program.

ix. Approve the resource requirement including Hardware / Software for Implementing Organization based on proposals submitted by them.

x. Approve the extension of Project within the Programme duration.

xi. Address any other issue required for smooth implementation of the program.

xii. Chairman of the NSC/GC (R&D in E) may invite / co-opt experts as and when required during the course of the Programme.

B. Technical Advisory Committee (TAC)

Technical Advisory committee would monitor the technical progress of the programme. The Chairman of the TAC would be member of the NSC and would apprise the NSC on the progress of the overall activity of the Programme. The other members of TAC would include

- Senior officials from Line Ministries/ Government Organizations.
- Experts from Academic institutes
- Experts from Renowned Research laboratories/Organizations
- Officials from User Agencies
- Experts from VLSI Industry/Association.

Terms of Reference of the Technical Advisory Committee

i. Review technical progress of Projects submitted by implementing organizations after the initiation.

ii. Recommend initiation of new activities and inclusion of new institutions as Participating Institutions in line with the aim of the project.

iii. Recommend the resource requirement including Hardware / Software of participating Institutions/Start-ups/MSMEs based on proposals submitted by them.

iv. Recommend the redistribution of funds among the different budget heads with in the approved budget outlay whenever necessary as per rules of MeitY.

v. Recommend the extension of Project within the Programme duration.

vi. Recommend any other related activity for smooth implementation of the project.

vii. Approve the proposals of Students/Researchers/faculty to attend and present the paper in International Conferences for the work carried out under the projects

xiii. The Chairman TAC/ GC (R&D in E) may co-opt/ invite expert for review as and when required during the course of the Programme.

C. Project Review and Steering Groups (PRSG)

The PRSG would periodically review the technical and financial project progress. The Chairman of the PRSG would be member of the TAC and would apprise the TAC about the project progress of implementing institutions.

For review & monitoring of category I project proposals, separate PRSG would be constituted. To review of category II & III project proposals, it is proposed to constitute thematic area wise PRSGs. Number of PRSGs would be decided based on the project proposals received in respective thematic areas.

The Chairman of the PRSG will have the option to invite Experts from Industry / Academic Institutes etc. during these PRSG meetings. PRSG would recommend release of funds to Participating Institutions/Start-ups/MSMEs. PRSG will also look into the aspect of re-distribution of funds and give its recommendation to TAC.

Terms of Reference of PRSG

i. To review the overall Technical and Financial progress of the Projects.

ii. To steer the projects from initiation to completion towards achieving specific output leading to useful outcome as per project objectives.

iii. To meet and visit the project sites as and when required to assess the progress made by the projects and to advice the project executing teams on new direction/approach and ensure its smooth progress and link-up with the work going on elsewhere in the country for full utilization of the capabilities available in the country.

iv. To examine specific request from Project Investigators, including re-appropriation of funds, enhancement of project outlay, change in the scope of the project, extension of project duration, change in the posts for project personnel, publication of research papers, provision for foreign travel, project completion report, equipment procurement, revision of bar/PERT chart, any other modifications and suggest remedial actions wherever required and make recommendations for consideration by MeitY

v. To advise action regarding completion of the projects, establishment of facilities, its utilization and transfer of know how etc.

vi. To review the Institutions for employability of manpower generated, absorbed by Semiconductor design houses, entrepreneurship culture resulted / inculcated as KPI (key performance indicator).

vii. Recommend the proposals of Students/Researchers/faculty to attend and present the paper in International Conferences for the work carried out under the projects.

viii. **Roadmap for translation:** PRSG should within 6 months of the commencement of the projects, discuss the need and the feasibility of translation/TOT of the proposed output of the projects for commercialization. If so feasible, PRSG should hold discussion with experts on the subject from Industry Associations, by inviting them especially to the meetings of the PRSG. PRSG, where possible, shall prepare a roadmap for translation/TOT for commercial production, keeping in view the extant guidelines in the matter.

ix. **Cost effectiveness:** PRSG should regularly review & guide the projects w.r.t. cost effectiveness of the technologies being developed under the projects where relevant. In case the Cost Benefit ratio, where relevant, is likely to be too adverse, PRSG may advise on mid-course correction or pre-closure of the projects. Recommend the redistribution of funds among the Institutions and also among the different budget sub heads with in the approved budget outlay in respective subheads whenever necessary as per rules of MeitY.

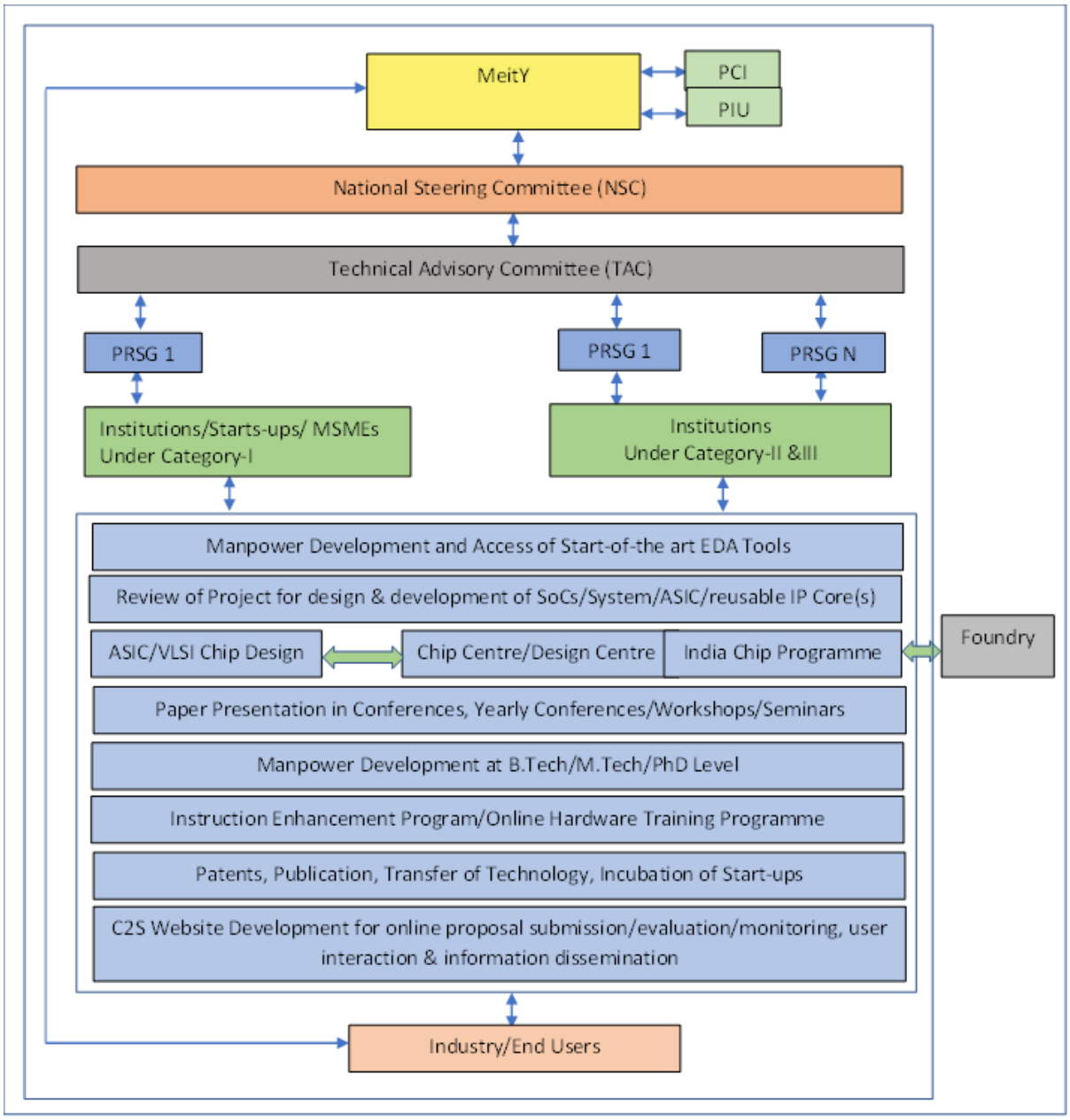
x. **Relevance of Technology to India:** PRSG should direct the projects efforts for development of globally competitive technologies with relevance to the Indian condition & requirements.

xi. The Chairman PRSG/ GC (R&D in E) may co-opt/ invite any other expert for review as and when required during the course of the Programme.

Since, the number of institutions involved in the programme is large, efforts would be made to evolve a self-monitoring mechanism by which the progress of each of the institute can be monitored efficiently and transparently.

The project performances would be reviewed by PRSG/TAC in the various review meetings organized periodically. The observations of PRSG and TAC would be placed before the NSC for approval. Based on the approval of NSC, MeitY would release the funds to CDAC, Bangalore (Programme Coordination Institute) for further release to all implementing institutions under the Programme.

The structure for implementing the Chips to Startupis shown below:



6.3.2 Travelling Allowance and daily Allowance for the Members of NSC, TAC and PRSG

The TA/DA to the Chairman, Members and Special Invitees of the NSC, TAC and PRSGs committee would be provided as per the GoI norms.

In addition to this, the Chairman and member/Invitee attending the meetings would be given Honorarium as per DST approved norms.

6.3.3 Submitting Six Monthly Technical and Financial Progress

All the Participating Institutions/Start-ups/MSMEs will submit the Project Progress Report (every Six Month) to MeitY in the prescribed proforma of "Six Monthly Technical and Financial Progress" proforma of MeitY.

7.0 Chip Centre & Design Centre

Under Special Development Programme for Chips to System design (SMDP-C2SD), Chip Centre was established at C-DAC, Bangalore for undertaking Siliconization of ASICs/Integrated Circuits designed by the Participating Institution. Chip Centre was the nodal centre for integrating the designs received from institutions and sending them to SCL for fabrication in MPW mode. Chip Centre also facilitated the Institutions in packaging of bare dies received from SCL.

In order to provide exposure of complete VLSI design cycle to all Participating Institutions from specification to Fab tape out, it is proposed to upgrade the capability and responsibility of existing Chip Centre and to establish a design Centre as part of Chip Centre for providing design support to the Institutions and Start-ups for development of ASIC and FPGA based designs.

7.1 VLSI IC Design Flow

The process of VLSI chip development can be divided into VLSI design, Chip fabrication, Packaging and Post Silicon Validation (Testing and Characterization). VLSI chip fabrication process is highly sophisticated, expensive and largely automated, and the VLSI design holds the key to the success of the VLSI chip. Proficient and efficient adoption of EDA tools for the VLSI design process is essential for successful tape outs and post silicon chip. Figure 6.1 depicts the overall VLSI design flow from Specification to Chip / System.

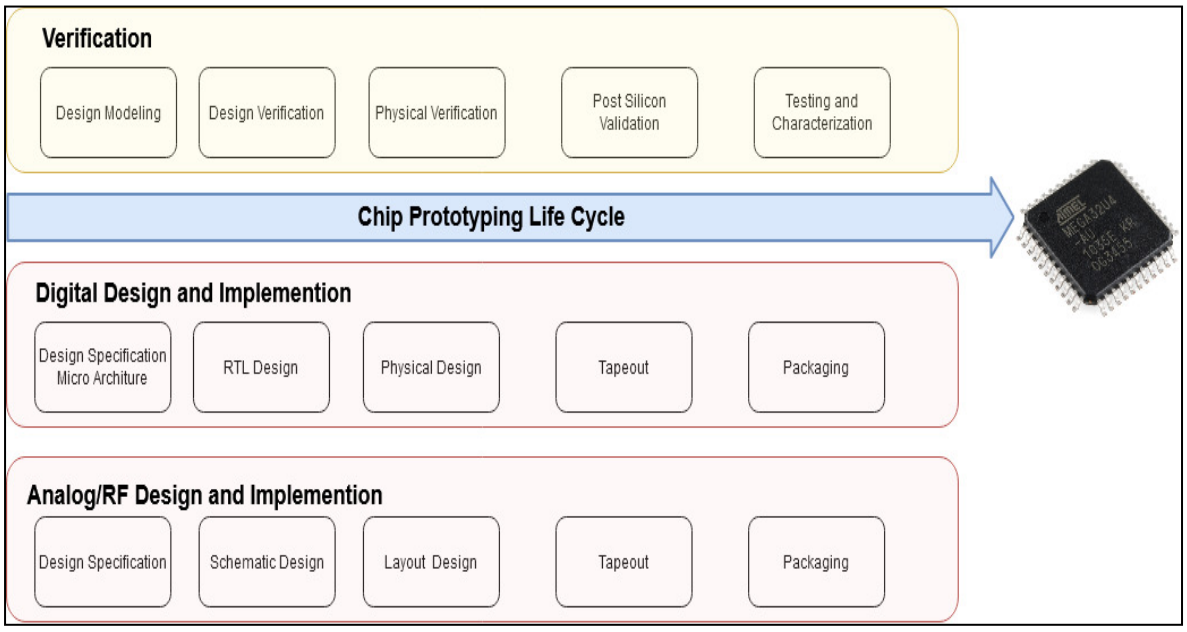


Fig. 7.1: VLSI Design Flow – Specification to Chip

VLSI design involves utilizing state-of-the art CAD / EDA tools, fab technology files, PDKs etc. and Chip fabrication uses advanced process tools / equipment and testing needs sophisticated test and characterization equipment.

The designs, particularly the digital designs, are done by writing hardware description of IC to be designed as RTL using the Hardware Description Languages – VHDL / Verilog / System Verilog / System C etc.

Typically, a digital design flow to get the end product is as follows:

Front-End (as depicted in fig 7.2(a))**:**

i. Formulation of functions & specifications of the proposed design
ii. Implementation of design / architecture – RTL coding
iii. Synthesis / Targeting to technology for RTL coding
iv. RTL Verification (functional as well as timing)

Back-End (as depicted in fig 7.3)**:**

i. Layout
ii. Functional and Timing Verification
iii. Physical Verification
iv. GDSII Tapeout to Foundry
v. Tape out to foundry for fabrication

For an analog design, the design flow (as depicted in fig 7.2(b)) may vary to some extent, i.e. specifications → architecture → circuit-design → SPICE-simulation → layout → parametric extraction / back annotation → final-design →Physical Verification→ (GDSII) tape-out for the foundry. While digital design is highly automated now, very small portion of analog design can be automated. Hence many analog chips are termed as 'flat' or non-hierarchical designs. This is true for small-transistor-count chips such as operational amplifiers, filters or power management chips. For more complex analog chips such as data converters, the design is done at the transistor level, building up to the cell level, then the block level and finally integrated at the chip level. SPICE remains the most useful simulation tool for analog as well as digital design.

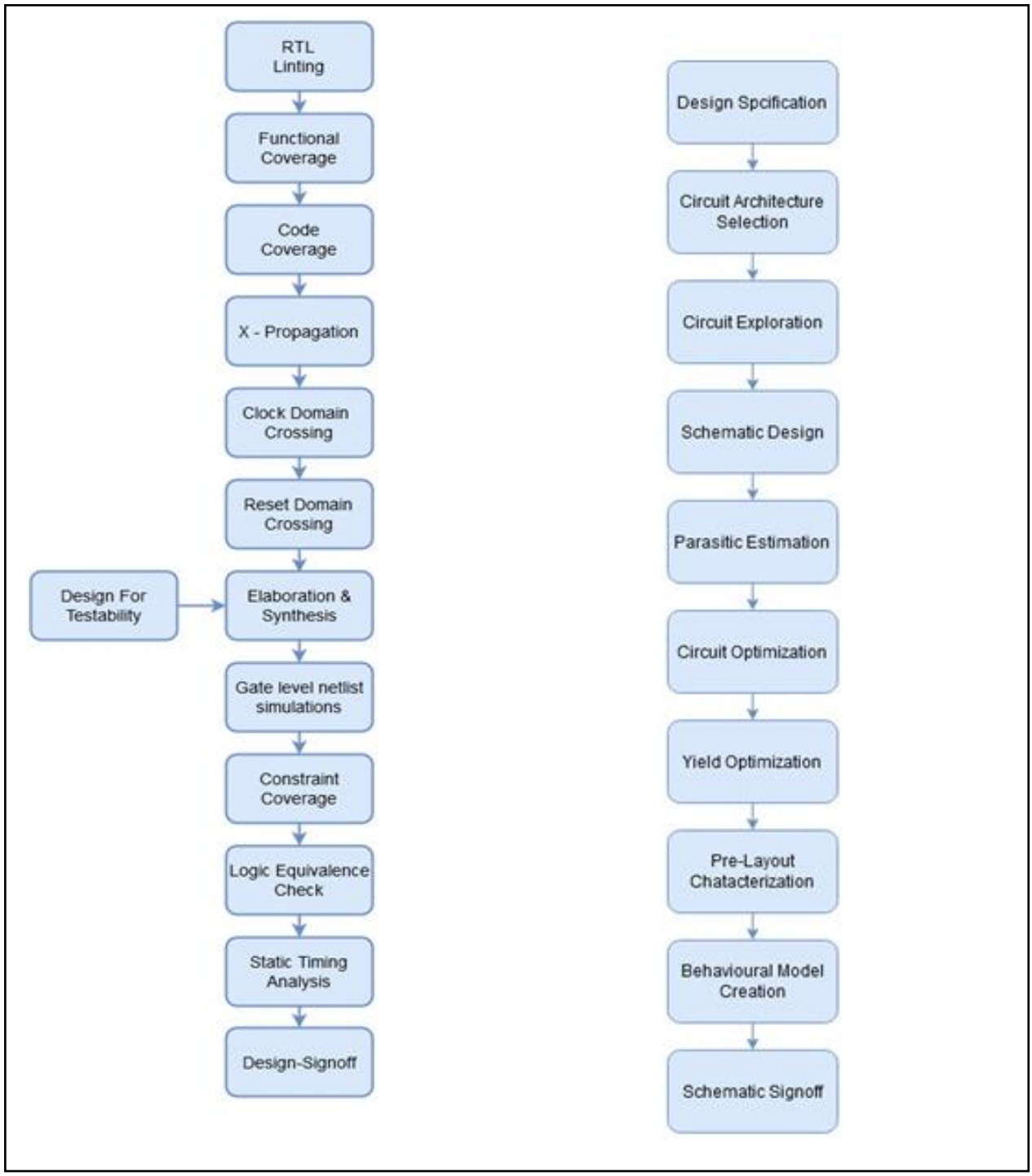


Fig. 7.2: (a) Digital Front-end Design Flow Fig. 6.2: (b) Analog Front-end Design Flow

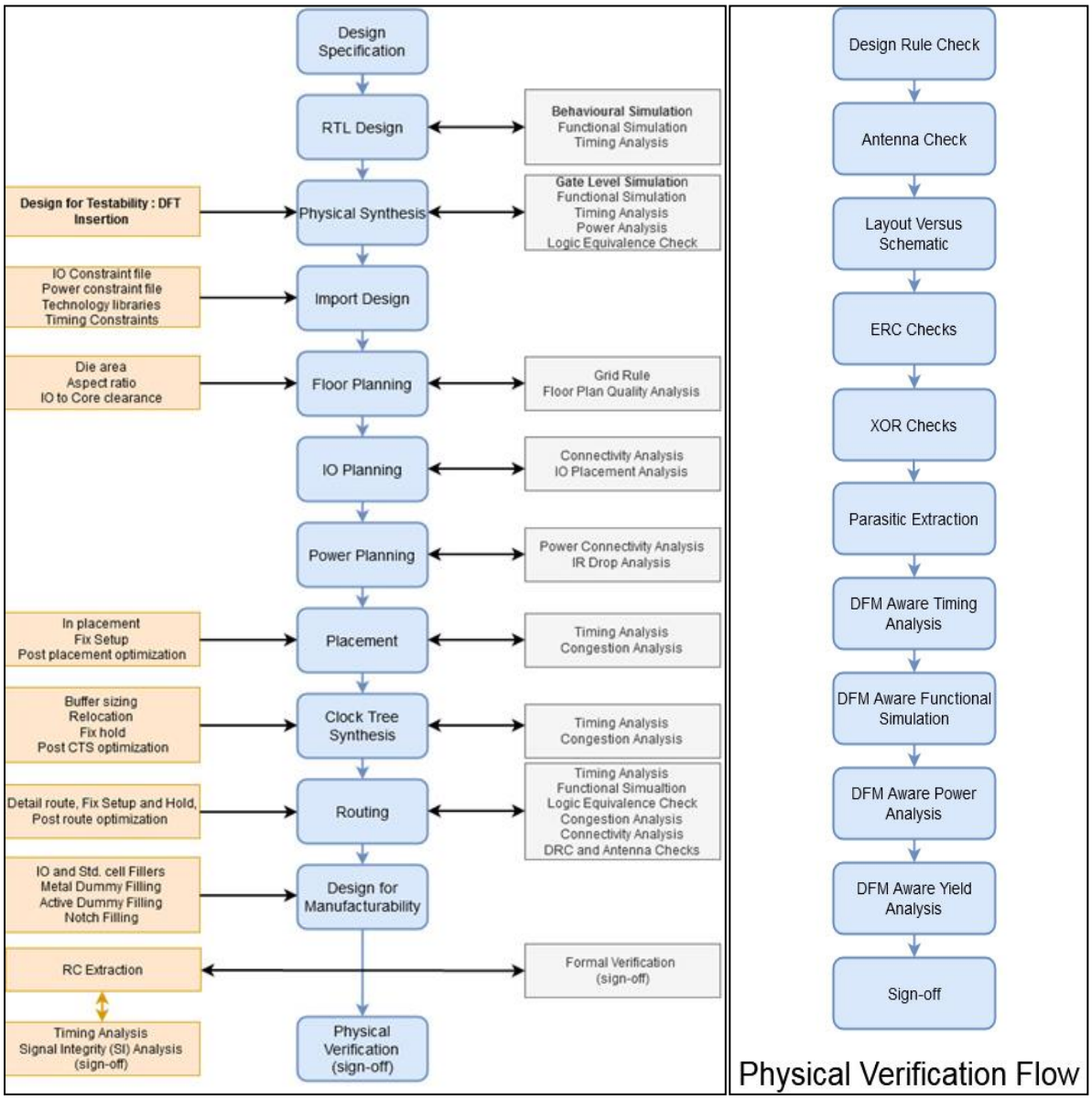


Fig. 7.3: Physical Design Flow – An Illustration

7.2 Upgradation of Chip Centre

Under C2S programme, it is proposed that Chip Centre would not only provide fabrication support at SCL and overseas foundries in MPW mode to Institutions/Start-ups/MSMEs but also offer design services including maintaining IP Core Repository, Design flow establishment with a specific set of EDA tools and the Fab PDK (as illustrated in figure 7.2 above), Fab compliance validation of Designs (as illustrated in figure 7.3 above), Packaging of Chips, Testing, Characterization in the Country in centralized manner.

Chip Centre would be involved in following activities:

Design Verification and Integration of Fab Compliant MPW Tape outs:
After completion ASIC design, Institutions would submit the GDSII to Chip Centre along with the design related information such as Tape out Submission form, Foundry Details, DRC report, Antenna Report, Device type used, List of legal layer used in the design, Stream out logs, third party IPs used details if any, and other required details. Besides, the Institutions would also provide the details related to the design tape out, packaging etc. to Chip Centre for integrating the different designs in single Reticle/Matrix.

Chip Centre would carry out necessary Physical Verification Checks (as depicted in figure 7.3) like DRC, LVS and Antenna Rules etc. The outcomes of the checks would be compared with the reports submitted by the Institutions and feedback would be given to the Institutions for design corrections, if required. Besides this, Chip Centre would also be carrying out other IC layout related checks to ensure the parameters of individual ASIC adhere to the Fab requirements. These checks would be performed on die size, design aspect ratio, dummy fill, seal ring, silicon number, I/O pads, bond pads and dimensions, bonding diagram and wires for feasibility / reliability, chip outer boundary scribe lines, pad ring, chip layers etc.

Further, on need basis, Chip Centre would guide the Institutions on the EDA tools usage / options for IC design with a specific Fab PDK, Standard Cell Libraries, Fab specific IC layout design requirements/parameters, layers design, memory tiles design spec. etc.

Only Fab compliant designs would be submitted by Chip Centre to Foundry. Once all the designs are verified against Fab specific IC tape-out criteria, Chip-Centre would carry out the floor plan of all the designs on a Reticle / block of suitable size as recommended by the Fab.

Fabrication Access at SCL and Overseas Foundries: like SMDP-C2SD programme, Chip Centre would integrate the designs of Institution targeted to SCL 180nm technology in single Reticle and send them to SCL for fabrication.

Chip Centre would also enable the access of overseas foundry viz. TSMC, UMC, Tower Jazz Semiconductoretc. to Institution and Start-ups through Chip Centre or through foundry support services like MOSIS, EUROPRACTICE (IMEC), and MUSE etc. in MPW mode depending on the need of the Project.

All the designs would be fabricated through Chip Centre on the supported technology nodes. Any special additional requirements for the institutes other than the proposed/supported foundry and technology nodes should be approved by PRSG/TAC/NSC and MeitY. In such cases, institutions are permitted to directly get the fabrication done through the fab / services. In such cases chip centre will not be involved in the task of fabrication and packaging for that particular tape out. Institutions will be requested and communicated to sign the NDA with inland and overseas foundry / foundry access provider to receive the PDK for various technology nodes supported through chip centre under the programme. Only institutions which had signed the NDA will be entertained for fab.

Chip Packaging: For the chips fabricated at SCL, Chip Centre would establish tie up with Chip Packaging and Assembly Unit for Back Grinding, Dicing, Wire bonding and Plastic packaging of IC. The packaged IC and bare dies would be sent to the Institutions. For the chips that are expected to be fabricated in overseas foundries, the suitably packaged chips and bare dies would be obtained from the respective foundry / foundry access provider / IC service unit and provided to the institutions.

Setting up a Repository of reusable IP Cores: Chip Centre would set up a Repository of reusable IP cores which could be made readily available for use by other designers/Participating Institutes. IP repository document would be developed by Institutions/Start-up/MSMEs based on template provided by Chip Centre. An 'on-line' data base of the designs available in the Repository would be made available at C2S website.

Facilitation for Patents/Copyrights and Trademarks for reusable IP Cores: Chip Centre would also facilitate the Participating Institutions to file Patents for the reusable IP Core(s).

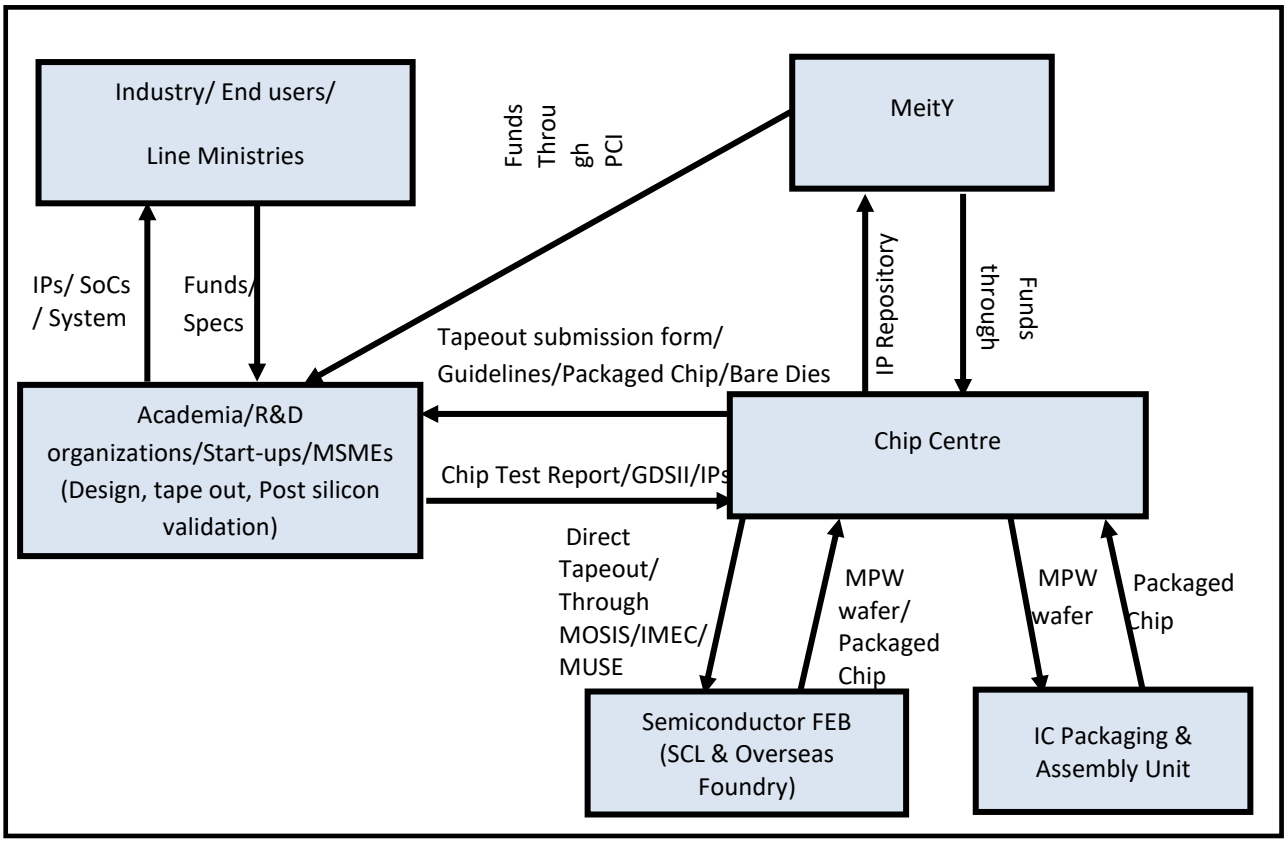


Fig. 7.4: Operational Model for Chip Centre

In summary broad responsibility of Chip Centre would be:

- Interaction with EDA vendors and establishing the requisite EDA tools for Full-custom IC design flow, Semi-custom or cell-based IC design flow, Analog / Mixed-Signal designs, SoC designs, etc.
- Distribution of latest design kits(PDKs), libraries and Memory cuts from Semiconductor foundry (through SCL, Mohali or any other foundry) to institutions under NDA control.
- Establishment of Design Flow with a specific set of EDA tools and the Foundry PDK by tape out of designs in respective node and foundry.
- Creation of reusable IP Core(s) Repository and facilitates the Institutions for Patent filing.
- Validation and Integration of designs received from various institutions and send to SCL for fabrication.
- Enabling the access to SCL and overseas foundries (TSMC, UMC, and Tower Jazz Semiconductor) through Chip Centre or through foundry support services like MOSIS, EUROPRACTICE (IMEC), and MUSE in MPW mode depending on needs/feasibility.
- Design and development of IPs / SoCs by Chip Centre for specific end applications in order to establish the design flow with identified foundries and deriving a design flow process for academia.
- Organizing training on EDA tools for the institutions as per the requirement and thereby giving exposure to them on the chip design cycle from specification to chip fabrication.
- Packaging of SCL fabricated Chips and Coordination with the Packaging Firm whenever required.
- Characterization and Prototyping Enablement.

7.3 Establishment of Design Centre

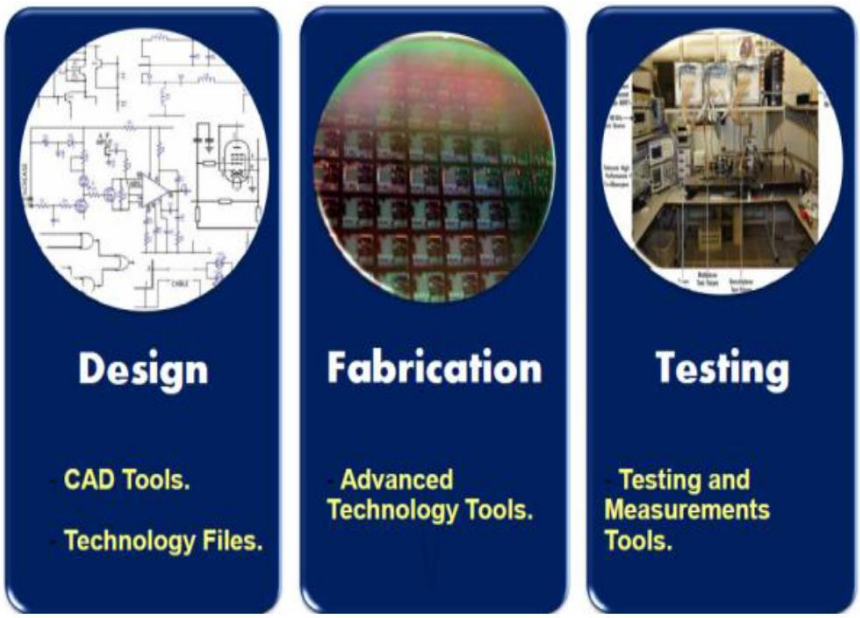
To streamline the adoption of a standardized VLSI design flow process among Academia/R&D Organization and Start-ups/MSMEs and for timely completion of design development, a Design Centre would be setup at CDAC Bangalore as a part of Chip Centre. Design Centre would be responsible for the following activity.

Handholding of New Institutions/Start-ups: Design Centre would be the nodal centre to handhold the new Institutions, category III SMDP-C2SD Institutions and Start-ups for development of ASIC and FPGA based design by organizing IEPs/Workshop/Training Programme through NIELIT Calicut.

Review of project proposals received from Academia/R&D Organizations /Start-ups/MSMEs under C2S: Under C2S, the Institutions/Start-ups/MSMEs would submit the proposals under three categories viz. Category I, II, and III. These proposals would be reviewed by Design Centre in association with MeitY before submitting to evaluation

Committee, if need arises Design Centre would guide the Institutions to revise / amend the proposals suitably, and such assistance may be a need for the new institutions which will enable to finalize the proposal better and be accommodated under the programme.

Creation of Design flow Guidelines / Best-Practices / Checklists / Report Templates: Development and manufacturing of VLSI Circuits involves three stages: Design, Fabrication and Testing.



At Design Stage, designer need to follow certain design guidelines and different steps of implementation as depicted in Figure 7.1 and 7.2 for ensuring quality of design and simplification of verification process; Design Centre would be involved in the preparation of design flow guidelines / checklists / report templates which would have to be adopted and adhered by designers while developing the IPs / ASICs / SoCs in their institutes. Abiding by such checklists, guidelines and best-practices during the VLSI design phase would improve yield results during Physical Design phase and would translate to reusable IPs for future designs.

- Guidelines / best-practices / standard for the following design process flow:

  - HDL coding guidelines and standard – Verilog / System Verilog / VHDL.
  - Effective test bench creation guidelines and best-practices.
  - FPGA prototyping guidelines.
  - IP / External / Internal interface standardization for “Design Reuse” and integration.
  - Design Process flow standardization – from design specification to GDSII tape out.

- Front-End and Backend Checklist. This would include the following:

- Linting and HDL checks.
- Functional Coverage.
- Code Coverage.
- X-Propagation Checks.
- Cross-Domain-Clock (CDC) checks.
- Gate-level Simulation with SDF.
- Constraint Coverage.
- Logic Equivalence Checks Pre and Post Layout.
- Static Timing Analysis (STA) Pre and post layout.
- Design for Testability (DFT).
- Elaboration and Synthesis checklist – FPGA / ASIC.
- Layout
- Post Layout Simulation
- Physical Verification
- Design Signoff (GDSII)

- Simulation Reports – Template and Reviews.
- Synthesis/Automatic Place and Route Reports – Template and Reviews.

Design Centre would be involved in the review of every stage of the design cycle (Coding / Schematic, Simulation, Synthesis, layout etc.) to ensure that timely corrections and revisions of the designs.

Coordinate/organize Workshop/Training Programme: Design Centre would handhold the new Institutions/Start-ups by conducting training programmes/workshops. Such Training Programme/Workshops by Design Centre would be held via webcast leveraging National Knowledge Network (NKN). Efforts would be made by Design Centre to rope in industry experts wherever required. The IEP/Workshop/training programme would focus on following:

- Design flow aspects: generation of golden RTL from design specification.
- Front-end design issues and mitigation.
- Functional Simulation, Coverage, Gate-level simulation (back-annotation with SDF).
- Synthesis – FPGA / ASIC.
- Layout
- Physical Verification

- Design Signoff (GDSII)
- Prototyping on PCI based FPGA development / evaluation boards.

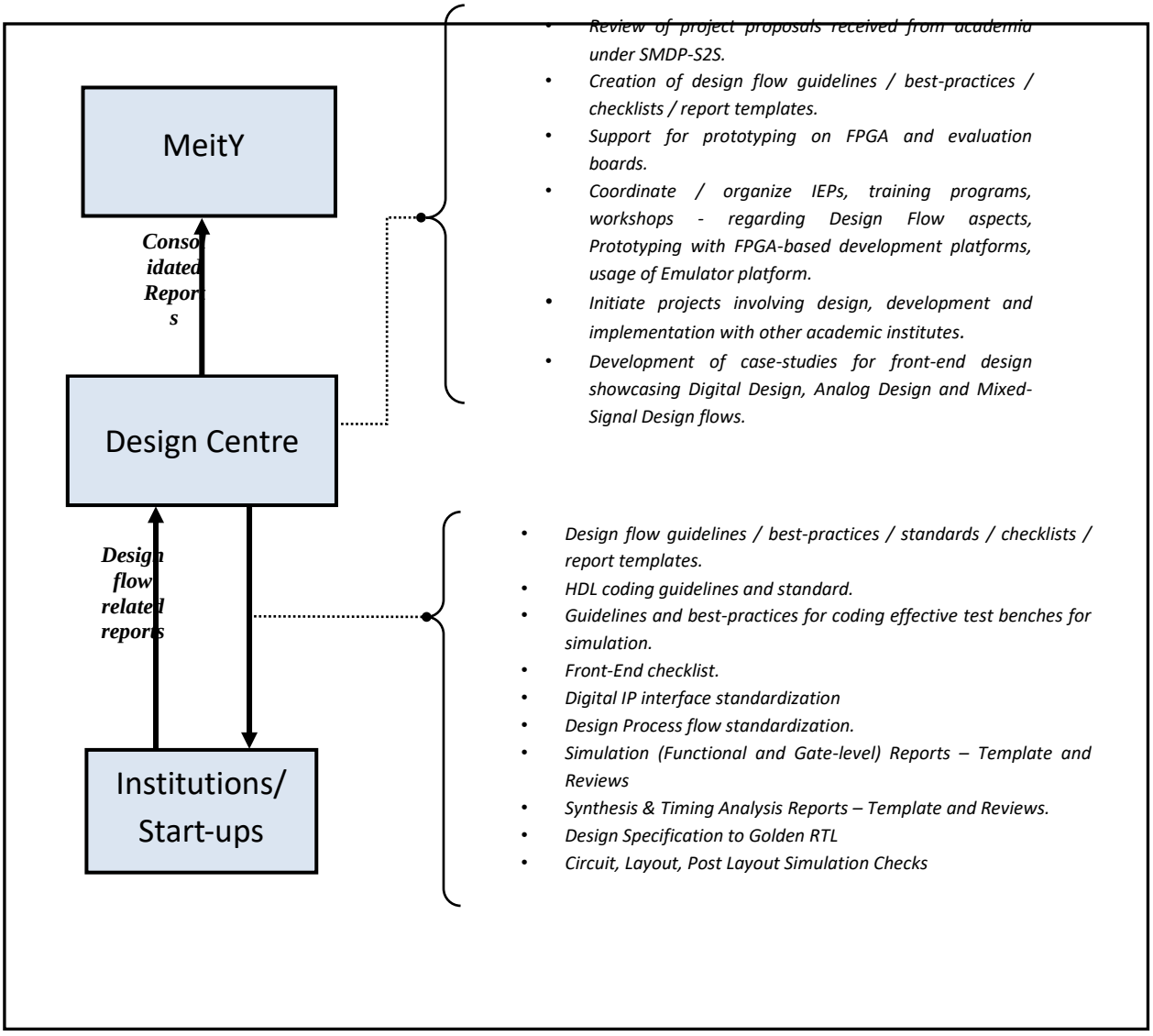


Fig. 7.5: Operational Model for Design Centre

In summary, the broad responsibilities of Design Centre would be:

i. Review of project proposals received from academia/R&D organizations/Start-ups/MSMEs under C2S.

ii. Handholding of New Institutions, Category III SMDP-C2SD Institutions /Start-ups for development of ASIC and FPGA based design project by providing design guidelines, technical interactions and checklists.

iii. Preparation of Design flow guidelines / checklists / report templates to be followed by designers for IPs / ASICs / SoCs. Such guidelines would have to be adopted by the institutes to enable standards-based design approach and “Design Reuse”.

iv. Coordinate / Organize training programs, workshops for Institutions/Start-ups to enhance the competency level of students/researchers.

v. Development of case-studies for front end design w.r.t. Digital Design, Analog Design and Mixed-Signal Design flows.

vi. Design Centre would also initiate projects involving design, development and implementation with other academic institutes, such as IISc/ IITs / NITs / etc. This could possibly be targeted towards specific applications areas.

vii. Any other design related activity.

7.4 Chip Centre and Design Centre Budget Heads

Year wise budget for Chip Centre including the Design Centre activities is as follows:

(Rs. in Lakh)

#	Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
1	Capital Equipment (including FE Comp.)	35.00	25.00	15.00	15.00	10.00	100.00
2	Consumables (including FE Comp.) *	30.00	40.00	48.00	42.00	40.00	200.00
3	Manpower	114.00	121.00	129.00	138.00	147.00	649.00
4	Travel & Training (including FE Comp.)	5.00	5.00	4.00	3.00	2.00	19.00
5	Contingencies	2.00	4.00	4.00	3.00	2.00	15.00
6	Overheads, if any	4.00	3.00	3.00	3.00	4.00	17.00
Total		**190.00**	**198.00**	**203.00**	**204.00**	**205.00**	**1000.00**

8.0 Financial Details

Total Outlay of C2S Programme would be **Rs. 250.00 Crore** for duration of **5 Years**.

The following are the broad budget heads under the Programme:

1. Category I Projects (including Academia-Industry Collaborative Projects/Grand Challenges/Hackathons/RFP for development of System/SoC/ASIC/IP Core under Category-I)
2. Capital Equipment (Access of EDA tools, Compute Infrastructure, FPGA Boards for design of System/SoC/ASIC/reusable IP Core(s))
3. Setting up Project Coordination Institute (Administrative and technical support to Programme Division of MeitY for overall Implementation of Programme and C2S website development)
4. Chip Centre (Nodal Centre for Integrating design of Participating Institutions at SCL foundry and enabling the access to outside Foundry)
5. IEP/Online Hardware Training Programme/Workshops/Symposium etc (Organizing IEP/Hardware training Programme/Workshops/Conferences/Symposium/Paper presentation in International Conferences etc)
6. Category II & III Projects (including India Chip Programme, Consumables, Travel & Training, Contingencies, Miscellaneous, Overheads Manpower/ Consumables/ Travel & Training/ Contingencies/ Miscellaneous/ Overheads) for implementation of Category-II & Category-III Projects,

The Head-wise and year-wise budget distribution between various heads of Programme is tabulated below:

8.1 Head-wise Breakup of total outlay

(Rs. in Crore)

#	Budget Head	Budget		
		(GEN)	**(NE)***	**Total**
1	Category-I Projects (including Academia-Industry Collaborative Projects/Grand Challenges/ Hackathons/RFP for development of System/SoC/ ASIC/IP Core(s))	70.00	0.00	70.00
2	Capital Equipment	63.00	2.00	65.00
3	Programme Coordination Institute (PCI)	6.00	0.00	6.00
4	Chip Centre	10.00	0.00	10.00
5	IEP/Online Hardware Training Programme/Workshops/Symposium etc.	5.75	0.00	5.75
6	Category- II & III Projects(including India Chip Programme, Consumables, Travel & Training, Contingencies, Miscellaneous, Overheads)	86.25	7.00	93.25
	Total Budget	**241.00**	**9.00**	**250.00**

*** Rs. 9.00 Crore has been provisioned for 8 NITs from North Eastern region. In addition, Design infrastructure support (EDA tools, Fabrication, Chip Centre, PCI and Training etc.) would also be made available to all North Eastern Institutions.**

The entire Grant-in-aid from MeitY would be released to CDAC Bangalore, Programme Coordination Institute (PCI) for distribution of funds to Participating Institutions/Start-ups/MSMEs and NIELIT Calicut for conducting IEP/Training Programme etc.

8.2 Year-Wise Breakup of Budget Heads

(Rs. In Crore)

Budget Head	1st Year		2nd Year		3rd Year		4th Year		5th Year		Total	
	GEN	NE	GEN	NE	GEN	NE	GEN	NE	GEN	NE	GEN	NE
Category - I Projects (including Academia-Industry Collaborative Projects/Grand Challenges/ Hackathons/RFP for development of System/ SoC/ASIC/IP Core(s))	17.00	0.00	15.00	0.00	15.00	0.00	14.00	0.00	9.00	0.00	70.00	0.00
Capital Equipment	34.50	1.50	14.50	0.50	5.00	0.00	5.00	0.00	4.00	0.00	63.00	2.00
Programme Coordination Institute (PCI)	1.07	0.00	1.12	0.00	1.18	0.00	1.27	0.00	1.36	0.00	6.00	0.00
Chip Centre	1.90	0.00	1.98	0.00	2.03	0.00	2.04	0.00	2.05	0.00	10.00	0.00
IEP/Online Hardware Training Programme/ Workshops/Symposium etc.	2.55	0.00	0.95	0.00	0.95	0.00	0.95	0.00	0.35	0.00	5.75	0.00
Category - II & III Projects including India Chip Programme, Consumables, Travel & Training, Contingencies, Miscellaneous, Overheads	15.25	1.20	16.15	1.30	17.15	1.40	18.25	1.50	19.45	1.60	86.25	7.00
Total	**72.27**	**2.70**	**49.70**	**1.80**	**41.31**	**1.40**	**41.51**	**1.50**	**36.21**	**1.60**	**241.00**	**9.00**
Grand Total	**74.97**		**51.50**		**42.71**		**43.01**		**37.81**		**250.00**	

8.3 The financial details of the C2S programme are elaborated in detail under the following various budget heads:

8.3.1 Academia- Industry Collaborative Projects/ Grand Challenges/ Hackathons/RFP

Under Category-I, minimum 15 Projects would be initiated under Academia-Industry Collaborative Projects/Grand Challenges/ Hackathons/RFP. The budget provision of Rs. 70.00 Crore has been kept for carrying out these activities. Fabrication support for Academia-Industry Collaborative Projects would be provided from design Infrastructure Support.

8.3.2 Capital Equipment

It is proposed to keep budget of Rs. 65.00 Crore for making available the following HW/SW infrastructure to the 100 Participating Institutions, Start-ups and MSMEs

i. Access of centralized state-of-the-art EDA tools facility (having EDA tools from Mentor Graphics, Synopsys, Cadence) for designing of Chips.

ii. FPGA boards (Xilinx) for early prototyping and embedded software development

iii. Compute Infrastructure for simulating designs.

iv. Workstations/Servers for 8 North eastern NITs (Rs. 25 lakh/per institute amounting to Rs. 2 Crore). Separate provision of Capital Equipment for NE Institutions has been kept for upgradation of the VLSI lab facility setup at these institutions during SMDP-C2SD Programme.

8.3.3 Project Coordinating Institute (PCI)

Project Coordination institute (PCI) at CDAC, Bangalore for regular monitoring and review of the technical & financial activities as well as providing administrative support to the Program Division, MeitY. The following is the cost estimates for 5 Years:

(Rs in lakh)

#	Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
1	Capital Equipment	8.00	4.00	2.00	2.00	2.00	18.00
2	Consumables	2.00	2.00	3.00	2.00	1.00	10.00
3	Manpower	59.00	65.00	71.00	78.00	86.00	359.00
4	Travel & Training	2.00	2.00	1.50	1.50	1.00	8.00
5	Contingencies	2.00	2.00	2.00	2.00	2.00	10.00
6	Website Development & Maintenance	6.00	6.00	6.00	6.00	6.00	30.00
7	PIU at MeitY	25.21	27.37	29.76	32.39	35.27	150.00
8	Overheads, if any	3.00	3.00	3.00	3.00	3.00	15.00
Total		**107.21**	**111.37**	**118.26**	**126.89**	**136.27**	**600.00**

8.3.4 Chip Centre

Chip Centre would not only provide fabrication support to all implementing institutions at SCL and overseas foundries (TSMC, UMC, Tower Jazz Semiconductor etc.) in MPW mode but also offer design services including maintaining IP Core Repository, Fab compliance

validation of designs, design flow establishment with a specific set of EDA tools and the Fab PDK, Packaging of Chips, Testing, Characterization in the Country in centralized manner.

The Design Centre would be a nodal centre in the Country who will be handholding the new Institutions/Start-up participating under the Programme for their ASIC and FPGA based designs.

Year wise budget for Chip Centre including the Design centre activities is as follows:

(Rs. in Lakhs)

#	Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
1	Capital Equipment (including FE Comp.)	35.00	25.00	15.00	15.00	10.00	100.00
2	Consumables (including FE Comp.) *	30.00	40.00	48.00	42.00	40.00	200.00
3	Manpower	114.00	121.00	129.00	138.00	147.00	649.00
4	Travel & Training (including FE Comp.)	5.00	5.00	4.00	3.00	2.00	19.00
5	Contingencies	2.00	4.00	4.00	3.00	2.00	15.00
6	Overheads, if any	4.00	3.00	3.00	3.00	4.00	17.00
Total		**190.00**	**198.00**	**203.00**	**204.00**	**205.00**	**1000.00**

8.3.5 IEP/Online Hardware Training Programme/ Workshops/Symposium etc.

It is proposed to keep **Rs. 5.75 Crore** for organising (a) Instruction Enhancement Program (IEP) (b) Online Hardware training Programme (c) Workshops/Symposium/ Conference etc in the area of VLSI and Embedded Design (d) providing support to Students/Researchers/Faculty of Institutions to attend and present the paper in International Conferences for the work carried out under the projects.

A. Instruction Enhancement Program (IEP)

It is proposed to keep **Rs. 1.0 Crore** for organising 3-4 IEPs per year totalling to 20 IEPs in the area of VLSI and Embedded Design over the duration of 5 Years.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
EPs	0.2	0.2	0.2	0.2	0.2	**1.0**

B. Online Hardware Training Programme through SMART Remote Lab Facility in VLSI and Embedded System

It is proposed to provide **Rs. 4.00 Crore** to set up a Skilled Manpower Advanced Research and Training (SMART) remote lab facility at NIELIT Calicut to train the 1 lakh students over a period of five years and to handhold Start-ups.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Online hardware training Programme through SMART Remote Lab Facility	2.2	0.6	0.6	0.6	0.0	**4.00**

SMART Remote Lab Budget Heads

(Rs. In Lakh)

Head	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment Rs. FE Comp.	160.00	0.00	0.00	0.00	0.00	160.00
Consumable stores Rs. FE [Comp]	12.00	8.00	4.00	2.00	0.00	26.00
Manpower	36.80	40.40	44.15	48.68	0.00	170.03
Travel & Training Rs. FE Comp.	4.00	4.00	4.00	1.00	0.00	13.00
Contingencies	1.00	1.00	1.00	1.00	0.00	4.00
Overheads, if any	6.12	6.66	7.22	7.45	0.00	27.45
Grand Total (FE Comp.)	**220.00**	**60.00**	**60.00**	**60.00**	**0.00**	**400.00**

C. Budget provision of Rs. 75.00 lakh (15 lakh per year) has been kept for organizing Workshops/Symposium/ Conference etc in the area of VLSI and Embedded Design and for providing support to Students/Researchers/Faculty of Institutions to attend and present the paper in International Conferences for the work carried out under the projects.

8.3.6 Category II & III Projects (including India Chip Programme, Consumables, Travel & Training, Contingencies, Miscellaneous, Overheads

Budget provision of Rs. Manpower/ Consumables/ Travel & Training/ Contingencies/ Miscellaneous/ Overheads budget head has been kept for the following activities

i. Implementation of Category-II & Category-III Projects

ii. India Chip Programme to provide fabrication support at overseas foundry

iii. Other activity of the Programme

a) Organizing PRSG/TAC/NSC meeting, honorarium Charges to review committee members

b) Third party evaluation of the Programme

c) Filing of patents for protection of design/technology to be developed under the Projects

8.3.5.1 Implementation of Category-II & III Projects

Under the Programme, 40 Institution would be included in Category-II and 50 Institutions in Category-III. It is proposed to provide financial support of **Rs. 81.4 Crore** to Category-II &III institutions as per following breakup:

a) Total Rs. 38.40 Crore (Rs. 96.00 lakh per institutions) over the duration of 5 Years to Category-II Institutions for development of application oriented working Prototype of IP Core(s)/ASICs/SoCs

b) Total Rs. 43.00 Crore (Rs. 86 lakh per institutions) over the duration of 5 Years to Category-III Institutions for proof of concept oriented research and development of ASICs/FPGAs

8.3.5.2 India Chip Programme

Under India Chip program, fabrication support would be provided to the implementing organizations for Chip fabrication at overseas foundries.

(Rs. in Crore)

Activity	**1st Year**	**2nd Year**	**3rd Year**	**4th Year**	**5th Year**	**Total**
Chip fabrication at the foundry @ Rs. 10-50 Lakhs for 4-20 tape out per year x 5 years	2.0	2.0	2.0	2.0	2.0	**10.00**

The details of budget requirement for Chip fabrication including targeted numbers have been estimated based on the project requirement including selection of foundry/ technology node.

8.3.5.3 For other activity of the programme including PRSG/TAC/NSC meeting, honorarium Charges to review committee members, Filing patents and third party evaluation **Rs. 1.85 Crore** has been provisioned under the Programme.

8.3.5.4 Budget Estimation for Manpower/Consumables/Contingency/Miscellaneous/ Overhead

Following are the approximate budget estimation for Manpower, Consumables, Contingency, Miscellaneous and Overhead budget heads

Manpower

The following is cost estimates of Manpower for Participating Institutions:

(Rs in lakh)

Manpower for Participating Institutions under Category-II						
Type	**1st Year**	**2nd Year**	**3rd Year**	**4th Year**	**5th Year**	**Total**
Project Associate – II (1 No) (@ Rs 0.45 lakh per month (35,000+HRA) +10% increment per annum)	5.40	5.94	6.54	7.20	7.92	33.00
Senior Project Associate (1 No) (@ Rs 0.54 lakh per month (42,000+HRA) +10% increment per annum)	6.48	7.13	7.85	8.64	9.51	39.61
Total	**11.88**	**13.07**	**14.39**	**15.84**	**17.43**	**72.61**
Total (for 40 Institutions)	**475.20**	**522.80**	**575.60**	**633.60**	**697.20**	**2904.40**

(Rs in lakh)

Manpower for Participating Institutions under Category-III						
Type	**1St Year**	**2nd Year**	**3rd Year**	**4th Year**	**5th Year**	**Total**
Project Associate – I (1 No) (@ Rs 0.40 lakh per month (31,000+HRA) +10% increment per annum)	4.80	5.28	5.81	6.39	7.03	29.31
Project Associate – II (1 No) (@ Rs 0.45 lakh per month (35,000+HRA) +10% increment per annum)	5.40	5.94	6.54	7.20	7.92	33.00
Total	**10.20**	**11.22**	**12.35**	**13.59**	**14.95**	**62.31**
Total (for 50 Institutions)	**510.00**	**561.00**	**617.50**	**679.50**	**747.50**	**3115.50**

Note:- HRA has been calculated approx. 27%-30 % of Basic Salary

Total Manpower Cost for Category II & III Institutions): Rs. 60.199 Crore ~ Rs. 60 Crore

All the institutions participating under the Programme would, however, have the flexibility of employing manpower different from the one mentioned above / giving different salaries etc. within the Institute norms. This they could do within the total manpower budget per Institution mentioned above.

Consumables

Consumables @ Rs. 2 lakh per year per institutions would be provided to 90 Institutions totalling to Rs. 9.00 Crores over duration of 5 years for test board procurement/system integration/testing/field trials/certification etc.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Consumables (Rs. 1.8 Cr per year for 90 Institutions @ Rs. 2 Lakhs per year per institutions	1.8	1.8	1.8	1.8	1.8	**9.00**

Contingencies

Contingencies @ Rs. 1 Cr per annum are proposed to be kept for unforeseen expenses under the project and will include cost of filing of IPRs, convening PRSG, TAC and NSC meeting & honorarium to members of these committees and third-party evaluation etc. Thus, total of **Rs. 5.0 Crore** over a duration of 5 years are proposed to be kept for this activity

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Contingencies (Rs. 72 lakh per year for 90 Institutions @Rs. 0.80 Lakh per year per institutions and Rs. 18 lakhs per year for IPR, PRSG, TAC, NSC meeting & honorarium Charges, third party evaluation etc.)	0.90	0.90	0.90	0.90	0.90	**4.50**

Travel & Training

The funds for this activity will include travel of students/faculty of Institutions for PRSG/NSC/TAC meeting, training Programme/IEP etc. A total of **Rs. 6.75 Crore** are proposed to be kept for this activity.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Travel & Training (Rs. 135 lakh per year for 90 Institutions @ Rs. 1.50 Lakh per year per institutions	1.35	1.35	1.35	1.35	1.35	**6.75**

Miscellaneous

To keep abreast with technology / development / latest trends etc. in Microelectronics / VLSI / System on Chip (SoCs) / System Development there will be a definite requirement of providing resources such as Books, e-books, on-line video lectures, Journal subscription etc. particularly for new Institutions in category III. The Institutions could purchase these resources depending on their requirement. It is proposed to keep sum of **Rs. 50.00 Lakh** (@ Rs. 10.00 Lakh per annum) over a period of 5 years. Under this head, up to 50 Institutions would be provided funds of Rs. 20,000 per Institute per Year for purchase of Books, Journals, IEEE subscription etc.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Miscellaneous (up to 50 new Institutions (@ Rs. 20,000 per Institute per year) for purchase of Books, Journals, Reports, IEEE subscription etc.	0.10	0.10	0.10	0.10	0.10	**0.50**

Overhead Charges

It is proposed to keep sum **of Rs. 2.00 Crore** (@ Rs. 40.00 Lakh per annum) over a period of 5 years. Rs. 2 lakh per institute would be provided to 90 Institution as overhead charges over duration of 5 Years.

(Rs. in Crore)

Activity	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Overhead	0.40	0.40	0.40	0.40	0.40	**2.00**

PERT Chart of the C2S activities to be undertaken

Tasks	Months After issue of administrative approval for Programme Initiation				
	12	24	36	48	60
1. Call for Proposal, Proposal Submission, Approval & Execution for Industry-Academia Collaborative Projects targeting TRL 7 and above Category I Projects					
2. RFP for design & development of IP Core/System/SoC of National Importance					
3. Grand Challenge initiation and execution					
4. Call for Proposal, Proposal Submission, Approval & Execution for Projects under Category II & III					
6. Procurement of Hardware / Software / EDA Tools/FPGA Boards for design & development activity					
7. Setup Project Implementing Unit and Project Coordination Unit and further programme management and execution					
8. C2S Website Development and Maintenance					
9. Initiation of M.Tech program in VLSI /Embedded System at Institutions no having the M.Tech Programme					
10. Organise Instruction Enhance Programme/Hardware Training Programme/ Workshop/Conferences					
11. Specialized Manpower Generation at B.Tech/M.Tech/PhD Level					
12. Design & Development of System/SoC/ASIC/IP Core and FPGA based designs					
13. Patenting the Innovative / Research Publications of papers in Journals / conferences					

For activities (a) to (e)

14. Fabrication / Prototyping / Testing of Chips/ protection of IP Core, reference design etc. a. Chip Centre activities on tape out signoff and Design Integration. b. Design centre activities on process establishment and development of Checklist c. India Chip Programme and Chip fabrication for C2S institutions and other institutions. d. Setup a repository of proven designs					

Impact Assessment Report on SMDP-C2SD Programme by VLSI Society of India

IMPACT ASSESSMENT REPORT ON

SPECIAL MANPOWER DEVELOPMENT PROGRAMME FOR CHIPS TO SYSTEM DESIGN

(SMDP-C2SD)

Ministry of Electronics & Information Technology
Government of India

Prepared By

VLSI Society of India

July, 2021

TABLE OF CONTENTS

1. SMDP-C2SD Program Objectives

Moving up in value chain by initiating System development activities at Institutions, 3rd Phase of the Special Manpower Development Programme (SMDP III) was conceptualized by MeitY with an aim not only to develop specialized manpower in VLSI Design but also to develop Working Prototype of System-on-Chip/ System/Sub-Systems using the ASICs/ICs developed in-house.

An umbrella Programme entitled **"Special Manpower Development Programme for Chips to System Design (SMDP-C2SD)"** was initiated under 'Digital India Programme' in December 2014 with total outlay of Rs. 99.72 Crore at 60 academic/ R&D institutions spread across the Country including IITs, NITs, IISc, IIITs & other Engineering Colleges with an aim to train 50,000 number of specialized manpower in the area of VLSI design and inculcate the culture of System-on-Chip (SoC)/ System Level Design at Bachelors, Masters and Research level. The Programme duration was later extended by 23 Months up to November, 2021.

The following were the objectives of the Special Manpower Development Programme for Chips to System Design:

- To bring in a culture of System on Chip / System designing by developing working prototypes with societal applications
- Capacity building in the area of VLSI/ microelectronics and Chip to System development.
- To broaden the base of ASIC / IC designing in the country
- To broaden the R&D base of Microelectronics / Chip to System through Networked PhD program
- To promote 'Knowledge Exchange Program'
- Protection of Intellectual Property generated

Special Manpower Development Programme for Chips to System Design(SMDP-C2SD) was one of the initiative to address the implementation of the Human Resource Development strategies of the Ministry to (i) support creation of capacities within academic institutions to enhance production of adequate number of PhDs and post graduates for supporting the growth of chip design and embedded software and board/hardware design industry in the country and (ii) Extend the Special Manpower Development Program for Very Large Scale Integration (VLSI) chip design to include large number of colleges and students leveraging National Knowledge Network.

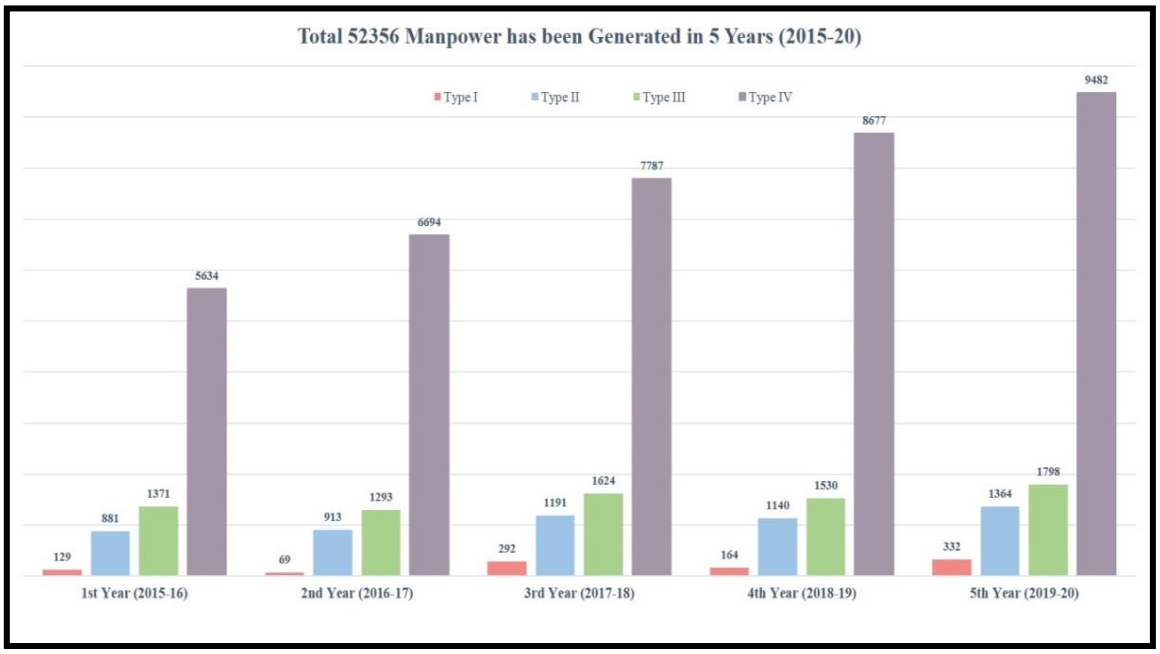
2. Major Achievements of the SMDP-C2SD Programme

2.1. Development of Specialized Manpower in VLSI/SoC/System/Sub-System Design

Under the programme, during first 5 Year of Programme, 52,365 no. of Industry ready Specialised Manpower has been generated in VLSI/ System Design Area at B.Tech, M.Tech and PhD level, which includes:

- Type-I (PhD)
- Type-II (M.Tech in VLSI),
- Type-III (M.Tech in Computer/ Communication etc. with at least two VLSI courses / minor project in VLSI)
- Type-IV (B.Tech with at least two VLSI Courses/ minor project in VLSI)

And other Students, who have utilized the VLSI Lab Resources created at Institutions under SMDP Programme.



Types of Manpower generated

#	1st Year (2015-16)	2nd Year (2016-17)	3rd Year (2017-18)	4th Year (2018-19)	5th Year (2019-20)	Total
Type I	129	69	292	164	332	986
Type II	881	913	1191	1140	1364	5419
Type III	1371	1293	1624	1530	1798	7556
Type IV	5634	6694	7787	8677	9482	38082
Total	**8015**	**8969**	**10894**	**11511**	**12976**	**52365**

Number of Manpower Generated

2.2. Establishing State–of-the art VLSI Design Laboratory

State-of-the-Art VLSI Design Laboratories were established at 60 Institutions equipped with Hardware platforms and Electronic Design Automation (EDA) Tools from Cadence/ Synopsys/ Mentor/ Xilinx. These labs are not only used by students involved under SMDP-C2SD project to undertake design of VLSI circuits but also by students from other Departments & nearby institutes.

2.3. Development of Working Prototype of Systems

Under the programme, inorder to inculcate the culture of Chip to System development activity at Institutions, 15 Systems/SoCs were undertaken by 10 RCs for development of Working Prototype. For each system project, End users were identified, and specifications were finalized in consultation with them. The End users were also involved in the Project Review Committee for continuous monitoring of the Project. These projects were also reviewed by the industry experts organized by IESA. The detailed list of the projects is attached in Annexure I.

2.4. Development of Applications Specific Integrated Circuits (ASICs) and board level designs using FPGAs

To provide the exposure of complete design cycle of Chip development, ASICs designs were also undertaken by Participating Institutions who were part of previous SMDP programmes. Under the Programme, total 150 ASIC were fabricated or being fabricated at SCL and outside. Detailed of number of ASICs developed by Different States and Institutions are given below. Additionally, 30 FPGA based board level designs were also undertaken by Category III institutions. Details of ASIC developed under the Programme are given at Annexure-II

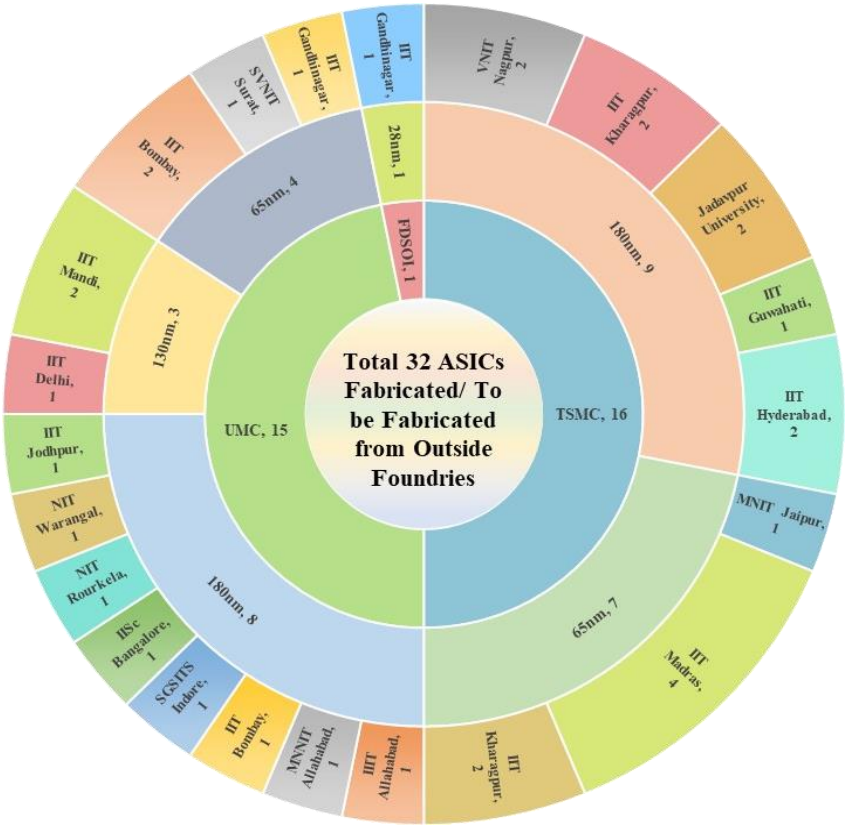
Total ASIC fabricated at SCL and outside foundries

2.5. Establishment of Chip Centre

For undertaking Siliconization of ASICs/Integrated Circuits designed by the Participating Institution, Chip Centre was established at C-DAC, Bangalore. Chip Centre is the nodal centre for integrating the designs received from Institutions and sending them for fabrication at SCL in MPW mode. Chip Centre also facilitated the Institutions for packaging of bare dies received from SCL. Under the Programme, through Chip Centre, 111 ASICs were fabricated and being fabricated at SCL in MPW mode. Chip Centre has also prepared the Checklists and templates to streamline the process of chip tape out at participating Institutions.

2.6. India Chip Programme

Under India Chip programme, ASICs fabricated by the Participating Institutions were supported for fabrication at overseas foundries in different technology nodes. Under India Chip Programme, total 32 designs were fabricated at outside foundry as depicted below



Total ASIC fabricated at outside foundry

Also, for providing fabrication support to Institutions who were not the part of SMDP-C2SD programme, Request for Proposal announced at MeitY and SMDP-C2SD website for selecting 10 best designs per year for fabrication at SCL Mohali.

2.7. Instruction Enhancement Program (IEP) to enhance faculty expertise in Microelectronics & Chip to System

Under the programme, 15 Instruction Enhancement Programme (IEPs) on different topics/area were conducted at various RC/PI locations by RCs and PIs for training faculty of Participating Institutions. A total of 1885 faculties/Lab Engineers of PIs were trained through this IEP. Details of various IEPs conducted are listed in the Annexure-III

2.8. Support for International Conference/Workshop

Under the programme, Researchers/Students of the 12 Participating institutions were supported for attending International Conferences and to present their work. Apart from this, 6 International Conference/Workshops were also supported in the area of VLSI/System under the programme.

Additionally, 5 ZoPP Workshop were conducted yearly for- reviewing the Project activities carried out by Institutions and working out Annual Action plan for all project implementing institutions & preparing Project Planning Matrix (PPM) for measuring the performance of the institutions. Details of various Conferences supported under the Programme are given at Annexure-IV

2.9. Patens/Publications

Under the Programme, 21 Patents have been filed by Participating Institutions in the area of VLSI/system design and about 1500 research papers published in reputed Conference Proceedings / Journals. Details of patents filed are listed in the Annexure-V

2.10. Development of Model Syllabus for B.Tech / M.Tech oriented towards SoC / System Designing and initiating M.Tech in VLSI / Embedded System Designing

With a view to promote System Designing in the country, a model syllabus/curriculum for B.Tech/M.Tech oriented towards SoC/System Designing including practical works/ minor projects etc. was prepared. The faculty of Resource Centres and other experts including experts from the industry was involved to work out the Model Syllabus. Efforts were made for adoption of this model syllabus curriculum oriented towards SoC / System Design in various institutions with the approval of their competent authorities which had facilitated the initiation of M.Tech in Microelectronics/VLSI design at 18 new participation institutions.

2.11. Involvement of Industry Associations and Experts

To ensure that the program deliverables meet the industry requirement, the industry experts involved at all the stages of the program. The experts were made members of the National Steering Committee (NSC), Technical Advisory Committee (TAC) and Project Review and Steering Group (PRSG). Also, experts from the industry were also involved in identification of SoC / system under the sub-activity 'Chip to System Development'. Whereas students from SMDP-C2SD institutions sent to leading Semiconductor MNCs (Intel/ NXP/ Cadence/Synopsys) for Internship of 6 months to 1 year duration throughout the programme.

2.12. Website Development and Web based dissemination of Educational Material

Under the programme, SMDP-C2SD website was developed by CDAC Delhi & being used to disseminate information including educational materials generated through IEP, Short-term courses, training programme on EDA tools, Review meeting, Information about Patent registered, Interactive forums to discuss design issues among researchers from 60 PIs. The URL for SMDP-C2SD website is **http://smdpc2sd.gov.in/**

3. Assessment:

Based on the objectives and goals of the SMDP-III, assessment across 12 different categories is presented in the following Matrix. Based on the evaluation and feedback received the SMDP-III program was a highly effective programme successfully met its objectives. Some of the areas where there is room for improvement are listed in the comments section of the table.

Goal	Target	Achieved	Grade	Comments
Manpower Development	50000	100%	A	Quality of the students could be better. Higher % of students in Type-I and Type-II should be targeted.
VLSI Design Laboratories	60	100%	A	Remote & Cloud based access to the infrastructure for Ease of access and better utilization of resources
Development of working prototype systems	15	15	B	Technical content and Commercialization potential could be improved by increasing effective industry participation.
ASIC and Board Level Designs Using FPGAs		Goals Achieved	B	Tape-Outs could have better and diverse technical &research contents to cater to wider range of applications
Establishment of Chip Centre		Goals Achieved	B+	Turn-around time for Tape-Outs was long and should be improved.
India Chip Program		Goals Achieved	B+	More Tape-Outs at Advanced Nodes as per need of the application.
Instruction Enhancement Program (Faculty Training)		Goals Achieved	B	Need more work; Trained and capable faculty is the key to success
International Conference Support		Goals Achieved	B	Bring and Support More International Conference in India. Increase student and faculty participation in international conferences abroad.
Patents and Publications (National, International)		Goals Achieved	A	H-Index and Citation Index need significant improvement
M. Tech & B. Tech Model Syllabus		Goals Achieved	B	Need AICTE approved B.Tech Program in Electronics & VLSI
Industry and Experts Involvement		Goals Achieved	B	Quality and Quantity of Industry and Global Experts needs improvement
Website Development		Goals Achieved	A	Good Start, device a way to collate all knowledge generated in a systematic manner.
Overall Score			8.83/10	

4. Recommendations

4.1. SMDP-IV: Continue and expand the next phase of the Programme

As the Semiconductor and Electronics industry is growing at a very fast pace, the demand for specialized manpower in VLSI Design, Device Technology and Semiconductor manufacturing processes is growing at a very fast pace. Considering this SMDP-IV should be expanded to more number of institutes and in next 5 years the program should target 100 Institutes and80,000 Special Manpower develop in various aspects of semiconductor industry. The number and percentage of students in Type I and Type-II should be increased to create a higher R&D impact.

4.2. Cloud based State-of-Art EDA & Design Tools Infrastructure

Build State-of-Art EDA Tools, Compute and Storage Infrastructure on the "Cloud" for R&D, Chip Development and Training. The Cloud based infrastructure will improve the ease and flexibility of access. Students, Faculty and Researchers will be able to access this infrastructure anytime from anywhere, thus better utilization of the available resources. This will also help in improving collaborative projects involving multiple institutes and industry partners. The Cloud based Tool Licenses, Compute and Storage has become industry standard practice and supported by all EDA Tools and other vendors.

4.3. Tape-outs and Working Silicon

SMDP-III did 111 Tap-Outs at SCL, Chandigarh and 32 ASICs at outside commercial foundries. In SMDP-IV program we should look at:

a. Similar to EDA tool vendors create a long-term contract with fab access providers like IMEC, Euro-practice or E-Fab type of entity to enable easy and economic access to the leading foundries, packaging and test services.
b. Plan for at least 50% of the Tape-out on the adequately advanced nodesat appropriate commercial foundries.
c. Many foundries are short of trained manpower to work in their manufacturing Fabs. It will be good to Create a two-way working relationship with leading one or more leading foundries, where the foundry provides the manufacturing services to the SMPD program participants and under the SMDP program we should provide trained people to work at these foundries.
d. In many cases the Tape-out (Shuttle Date) to Packaged sample time was more than 6 months, it is recommended to put the appropriate processes in place to have the samples ready in 4 months or less time period.

4.4. Faculty & Eco-System Development

As Faculty is cornerstone to success of SMDP programs, more focus should be done on faculty development, training and IEP program should be enhanced.

a. Frequent workshops including hands on lab exposure with participation from Industry should be conducted.
b. "Actively" participate and support international conferences in India such as VLSI-Design, ITC, VDAT, DVCON, Accellera-Day, ATS, ISCAS to increase international interaction and collaboration. Participation in International Conference of repute abroad such as ISSCC, CICC, ISLPED, DAC, DATE, ICCAD, IEDM may be targeted. 10-15 SMDP scholars/faculty members can be sent with partial travel/registration etc support from SMDP Program.
c. Faculty should be encouraged to spend 6 months in industry to understand the latest trends & technologies. The faculty may be asked to initiate a joint PhD guidance with the industry partner on a problem which is mutually decided.

4.5. Student Development & Training

a. For getting best of the talent interested in the field of VLSI and Semiconductors a new bachelor's program in Electronics and VLSI should be started in accordance with AICTE process.
b. Create a platform to provide internship opportunities for at-least 100 students per year at the leading semiconductor companies. An appropriate budget could be allocated to support this activity.
c. Ph.Ds in certain areas may be linked to compulsory industry internships.

4.6. Industry Collaboration

"Meaningful" Industry collaboration is key to success of the SMDP program. Following are few recommendations to create an effective collaboration between industry and academia.

a. Create an expert committee to understand the challenges and opportunities to enhance Industry academia collaboration in the area of Semiconductor and VLSI design and report their finding and recommendation in 6week after the committee is constituted.
b. Industry professionals should be encouraged to spend time in academic institutions. Most of the institutes now have "Professor of Practice" concept. We should leverage this and get at-least 10 industry experts as professor of practice at leading institutions.
c. For the technologies and projects targeted for commercialization and Start-up a relevant and interested industry partner should be mandated from beginning of the project. To make this effective the industry partner should provide minimum of 10% of the project cost as financial support.

4.7. Commercialization of Technologies and Start-ups support

There is immense potential of using the capabilities of the academic eco-system in collaboration with Industry to create Chip or Systems level products which require new concepts and significant R&D. The following are few recommendations in this area:

a. **Project based on the technologies developed in the academic institutes:** A quarterly review should be held for the technologies developed in the academic institutes where POC is done and the team is ready to take the technology to protype and commercialization. Based on these reviews 20 projects should be selected during the period of the program by an expert committee composed of industry experts. For the selected projects, an industry partner should be identified who is interested in commercialization of the technology and ready to provide minimum of 10% of financial support for the project. The expert committee should validate the capabilities and interest of the industry partner. These projects should result into viable products either at the chip level or at the system level.

b. **Projects based on National and Strategic priorities:** Projects and Products which are of national importance similar to NAVIC and India Microprocessor should be done by floating and RFP with the required specs and open to both industry and academia. The chosen entity should have a required technical expertise, right and sufficient resources and the track record for executing such projects. Five to ten such projects could be conceived and supported during the program. As these programs are time bound and of national importance, 2 experts should be assigned to each project for continuous involvements and project supervision on a regular basis. Some examples for such projects could be Apps Processor for Mobile phone and Tablets, Wi-Fi chip based on latest technologies such as Wi-Fi 6, Chip for Electronics Passports, Chip for Smart energy meters etc.

c. **Create strong linkage with National Fabless policy:** for the projects and technologies which are targeted for commercialization to create a continuum of technology development from academia to industry to successful and scalable companies.

d. A milestone-based planning and review mechanism linked with funding needs to be formed.

e. Start-up support through NIDHI/PRAYAS programme and TBI (in most of the Institutes) may be considered in the SMDP-IV program.

5. Acknowledgements

VLSI Society of India thanks to the VLSI Team and Review committee for their valuable suggestions and comments and would like to acknowledge the contributions of the following experts:

- Sumit Goswami, Qualcomm, VSI Steering Committee Member
- Preet Yadav, NXP, VSI Steering Committee Member
- Chitra Hariharan, Intel, Secretary VLSI Society of India
- Niranjan Pol, Seagate, Vice-President, VLSI Society of India
- Veeresh Shetty, Siemens, VSI Steering Committee Member
- Prof. V. Kamakoti, IIT Madras
- Mr. E. Magesh, Executive Director, C-DAC, Trivendram
- Prof. Sudeb Dasgupta, IIT Roorkee
- Mr. Ashok Mishra, VP, ACL Digital, GC Member SFAL
- Smt. Hemlata Gupta, Scientist ‘C’, Mr. Nishit Gupta, Scientist ‘D’ Meity
- Prof. Dinesh Kumar Sharma, IIT Bombay, Chairman Technical Advisory Committee
- Smt. Sunita Verma, Sr. Director Meity, and SMDP-C2SD program co-ordinator
- Dr. Abhijeet Karmakar, Sr. Principal Scientist, CEERI Pilani and PIU (Programme Coordinating Unit), SMDP-C2SD

Annexure I

#	System Project Title	RC	End User/ Application
1	ASIC for Next Generation LCA	IISc-B	ADA (DRDO) & ISRO
2	Integrated microchip module for wireless capsule endoscopy	IIT-D	Healthcare
3	Collision Detection in Automobiles using CMOS Imagers		Healthcare
4.	MAVI: Mobility Assistant for the Visually Impaired		Automotive
5.	Versatile Data Acquisition & Signal Processing Platform with specific emphasis on Seismic Application	IIT-Kgp	Disaster Management, MoES
6.	Design and Implementation of variable data rate (up to 10 GBPS) (SerDes Serializer/ Deserializer) system		ISRO and DRDO
7	Wireless Sensor Networks Node for Internet of Things (IoT)	VNIT-N	Railways
8	Versatile Physiological Signal Monitoring System	IIT-B	Healthcare
9	SerDes: High Speed Data Transceiver		SAC (ISRO)
10	Low Power Speech Recognition System using a custom IC	IIT-M	Consumer Electronics
11	UWB beam-forming Camera		Strategic
12	Wireless Sensor Node – System On Chip (WSN-SOC) for Monitoring of illegal activities	IIT-K	Forest Department of Odisha
13	RF Sensing of Cardiopulmonary Motion for survival detection under debris	IIT-R	NDRF Uttarakhand/ Disaster Management
14	System-on-Chip platform for Secured Speech Communication	CEERI	Strategic sector
15	FPGA/ASIC based Sensor Platform for Monitoring Air Pollutants	IIT-G	Assam Pollution Control Board

Annexure-II

Details of Applications Specific Integrated Circuits (ASICs) under SMDP-C2SD			
#	**Institute**	**Technology Node**	**ASIC/ Design Name**
1	CEERI Pilani	SCL 180 nm	Capacitor based DC-DC boost converter (Charge Pump), Inductor based DC-DC boost converter (Inductor is off-chip), and Regulator circuit.
2	CEERI Pilani	SCL 180 nm	Digital designs like encoder, decoder are present, whereas analog designs includes current to frequency converters. Designs make use of basic building block like inverters, common source amplifier, and level shifter circuits.
3	CEERI Pilani	UMC L130/L110AE Logic/Mixed-Mode/RF	SoC Consisting of Processor, Memory, Vocoder and Cipher engine.
4	IIT Jodhpur	SCL 180 nm	Phased Locked Loop (PLL)
5	IIT Jodhpur	SCL 180 nm	1 KB SRAM
6	IIT Jodhpur	SCL 180 nm	Design of Sensor Signal Conditioning System
7	NIT Kurukshetra	SCL 180 nm	AES Encryption Decryption block
8	NIT Kurukshetra	SCL 180 nm	A digitally controlled low dropout voltage regulator
9	NIT Hamirpur	SCL 180 nm	Vocoder using FS 1016 standard Verilog IP
10	NIT Hamirpur	SCL 180 nm	SRAM tile design
11	NIT Hamirpur	SCL 180 nm	Signal conditioning ASIC for the detection of combustible Gases
12	TIET Patiala	SCL 180 nm	Crypto Chip
13	TIET Patiala	SCL 180 nm	4-bit Flash ADC with Digital Comparator
14	TIET Patiala	SCL 180 nm	6-bit All Digital Flash ADC
15	IIT Delhi	SCL 180 nm	Image Compressor Transmission
16	IIT Delhi	SCL 180 nm	High Dynamic Range Imager
17	IIT Delhi	SCL 180 nm	Time of Light

18	IIT Mandi	SCL 180 nm	Analog signal processing hardware for an on-chip Electroencephalogram (EEG)
19	IIT Mandi	UMC 130 nm	Frequency Synthesizer
20	IIT Mandi	SCL 180 nm	Low bandwidth SAR ADC Filter
21	NIT Srinagar	UMC 130 nm	Power amplifier for capsule endoscopy
22	NIT Srinagar	SCL 180 nm	Arbitration Unit
23	IGDTUW Delhi	SCL 180 nm	Band Gap Reference Circuit
24	IGDTUW Delhi	SCL 180 nm	Wireless Endoscopy Transmitter
25	IIT Kanpur	SCL 180 nm	Wireless Sensor Node System On Chip (WSN-SOC)
26	IIT Kanpur	SCL 180 nm	50MHz Phase Lock Loop
27	IIT Kanpur	SCL 180 nm	Universal Asynchronous transmitter and receiver
28	MNNIT Allahabad	SCL 180 nm	Advanced Video Decoder for Mobile Telemedicine (AVDMT)
29	IIT Patna	SCL 180 nm	CI-OFDM baseband modulator and demodulator for DVB-SH-A standard
30	IIT Patna	SCL 180 nm	RISK-V Processor
31	IIT-BHU Varanasi	SCL 180 nm	Timer and Interrupt with Wishbone architecture
32	IIIT Allahabad	SCL 180 nm	PLL
33	IIIT Allahabad	SCL 180 nm	Receiver
34	IIIT Allahabad	SCL 180 nm	Low noise amplifier
35	IIIT Allahabad	SCL 180 nm	6-bit ADC for low power wireless sensor network
36	IIT Bhubaneswar	SCL 180 nm	Delta Sigma ADC and analog to information converter for wireless sensor node
37	IIT Bhubaneswar	SCL 180 nm	AIC for Audio Sensing
38	IIT Bhubaneswar	SCL 180 nm	PPG SoC
39	IIT Kharagpur	SCL 180 nm	RF Balun
40	IIT Kharagpur	SCL 180 nm	Antenna on CMOS chip

41	IIT Kharagpur	SCL 180 nm	Variable Gain amplifier based Analog Front End
42	IIT Kharagpur	TSMC 180 nm CMOS LP MS/RF	Co-design of On-chip antenna and Low Noise Amplifier at 2.4 GHz
43	IIT Kharagpur	TSMC 180 nm CMOS LP MS/RF	Multimodal Energy-Harvesting Chip
44	IIT Kharagpur	TSMC 180 nm	SerDes (up to 12 Gbps)
45	IIT Kharagpur	TSMC 65 nm	SerDes (up to 16 Gbps)
46	IIEST Shibpur	SCL 180 nm	Single channel 14-bit Single Ended SAR ADC
47	IIEST Shibpur	SCL 180 nm	Single channel 14-bit Fully differential SAR ADC
48	IIEST Shibpur	SCL 180 nm	3-channel 14-bit Fully differential SAR ADC
49	IIEST Shibpur	SCL 180 nm	Power Aware Reconfigurable ADC (8-22 Bit)
50	Jadavpur University	TSMC 180 nm	ASIC comprising of Frequency Synthesizer, LNA
51	University of Calcutta	SCL 180 nm	CMOS Design of Analog Front End
52	NIT Sikkim	SCL 180 nm	Class - C Power Amplifier
53	NIT Sikkim	TSMC 180 nm	Frequency Divider Chip
54	NIT Durgapur	SCL 180 nm	Design and implementation of Analog Front End
55	NIT Durgapur	SCL 180 nm	AFE for Seismic System
56	NIT Durgapur	SCL 180 nm	Temperature Sensor with built in ADC Design
57	IISc Bangalore	SCL 180 nm	Low power Analog data acquisition system for Light Combat Aircraft Applications
58	IISc Bangalore	UMC 180 nm	Low power wireless data acquisition system for Avionics Applications
59	NIT Warangal	SCL/ UMC 180 nm	On Chip LDO voltage regulator for mobile applications
60	PSGCT Coimbatore	SCL 180 nm	Serial Interface controller for crypto processor
61	NIT Rourkela	SCL 180 nm	MPPT Controller
62	NIT Rourkela	SCL 180 nm	Charge Pump for energy Harvesting

63	IIT Bombay	SCL 180 nm	Versatile Physiological Signal Monitoring System for Healthcare Applications
64	IIT Bombay	SCL 180 nm	Serializer Chip Control logic and 8B/10B Encoder
65	IIT Bombay	SCL 180 nm	Deserializer Chip Control logic
66	IIT Bombay	SCL 180 nm	Reference clock generators for the Tx and Rx (DAC, PLL,..)
67	IIT Bombay	SCL 180 nm	Loopback SerDes Chip and Device Characteristic test chip
68	SVNIT Surat	SCL 180 nm	Bio-signal Demodulator
69	SVNIT Surat	SCL 180 nm	Artefact Suppression
70	MANIT Bhopal	SCL 180 nm	Development of AES 128 Encryption/Decryption modules
71	MANIT Bhopal	SCL 180 nm	Development of Radiation Hardened by Design (RHBD)
72	IIT Indore	SCL 180 nm	SRAM Memory Design
73	IIT Indore	SCL 180 nm	8B/10B ENCODER - DECODER
74	IIT Gandhinagar	SCL 180 nm	Radiation-hard SRAM Memory and Logic Design
75	IIT Gandhinagar	UMC 65 nm	RadHard-by-Design Standard Cell Library
76	IIT Gandhinagar	SCL 180 nm	Low power High Resolution SAR ADC
77	SGSITS Indore	UMC L180 Mixed Mode/RF-1P6M-1.8V/3.3V	2.4 GHz Direct conversion RF Receiver
78	IIT Madras	TSMC 65 nm	Delta Sigma Audio ADC
79	IIT Madras	TSMC 65 nm	8-channel UWB Beam former
80	NIT Silchar	SCL 180 nm	Preamplifier Design of Neural Amplifier
81	NIT Silchar	SCL 180 nm	Preamplifier Design for Speech to Text Design
82	IIITDM Kanchipuram	SCL 180 nm	Feature Extraction Engine 8KHz
83	IIITDM Kanchipuram	SCL 180 nm	Feature Extraction Engine 16KHz
84	IIITDM	SCL 180 nm	Phase Locked Loop

	Kanchipuram		
85	IIITDM Kanchipuram	SCL 180 nm	Sigma Delta ADC Design
86	NIT Tiruchirappalli	SCL 180 nm	Speech Recognition - Search Engine Module
87	NIT Tiruchirappalli	UMC 180 nm	Wireless Transmitter and Receiver for low data rate applications
88	NIT Tiruchirappalli	SCL 180 nm	MFCC Based Feature Extraction Module
89	NIELIT Calicut	SCL 180 nm	Array Signal Processor
90	NIT Calicut	SCL 180 nm	OTA based high speed buffer for line drivers
91	NIT Calicut	SCL 180 nm	PLL for Clock Generator
92	NIT Arunachal Pradesh	SCL/TSMC 180 nm	Signal Conditioning Circuit
93	NIT Arunachal Pradesh	SCL 180 nm	8:1 Serializer circuit
94	NIT Meghalaya	SCL 180 nm	SAR-ADC
95	NIT Meghalaya	SCL 180 nm	High performance 64X6-bit content addressable memory
96	NIT Agartala	SCL 180 nm	16 - bit SAR ADC
97	NIT Agartala	SCL 180 nm	EDM Algorithm
98	NIT Agartala	SCL 180 nm	DC - DC Buck Converter
99	VNIT Nagpur	TSMC 180 nm	ADC for Analog Front End
100	VNIT Nagpur	SCL 180 nm	Wireless Sensor Network Node With ZigBee Standards
101	MNIT Jaipur	UMC 180 nm	Design and Implementation of Analog Front End
102	MNIT Jaipur	28-32 nm	Hardware Security for IoT odes using Physically Unclonable Function (PUF)
103	MNIT Jaipur	SCL 180 nm	Signal conditioning circuit
104	IIITDM Jabalpur	SCL 180 nm	Low power processor based power management unit for Internet of Things (IoT) applications
105	NIT Jamshedpur	SCL 180 nm	Design of ADC module for WSN n/w nodes for IoT

106	IIT Roorkee	IHP (Foundry) 130nm BiCMOS	Low noise amplifier (LNA) for S band
107	IIT Roorkee	0.25 umGaN on SiC	2.4 GHz 8-10 W Power Amplifier
108	IIT Roorkee	SCL 180 nm	Second order delta sigma ADC and dynamic comparator
109	IIT Roorkee	SCL 180 nm	Voltage controlled oscillator (nominal voltage + low voltage), latch and counter
110	NIT Goa	SCL 180 nm	10-bit SAR ADC
111	NIT Goa	SCL 180 nm	Design and Implementation of Standard cell based Flash 5 bit-ADC
112	NIT Jalandhar	SCL 180 nm	VCO Remote Detection of Humans Trapped Under Debris in Disaster Affected Areas Using RF Sensing of Cardiopulmonary Motion
113	NIT Jalandhar	SCL 180 nm	Low Power RF Mixer
114	PSGCT Coimbatore	SCL 180 nm	Serial Peripheral Interface Controller
115	NIT Jalandhar	SCL 180 nm	Ring VCO for detection of human trapped under Debris
116	NIT Goa	SCL 180 nm	10-BIT SAR ADC
117	NIT Silchar	SCL 180 nm	Microphone Preamplifier for Speech to Text
118	NIT Trichy	SCL 180 nm	Speech Recognition - Feature Extraction Module
119	IGDTUW	SCL 180 nm	Bandgap Reference Circuit
120	SVNIT, Surat	SCL 180 nm	Bio impedance Signal Demodulator
121	SVNIT,Surat	SCL 180 nm	ECG artefact suppression
122	NIT Calicut	SCL 180 nm	OTA based high speed buffer for line drivers
123	NIT Calicut	SCL 180 nm	PLL-based clock generator
124	IIT Jodhpur	SCL 180 nm	200MHz Phase Locked Loop and SRAM 1 KB combined chip
125	IIT Bhubaneswar	SCL 180 nm	Delta Sigma ADC design
126	MNIT Jaipur	SCL 180 nm	Hardware based Random Number Generator using PUF
127	NIT Trichy	SCL 180 nm	Speech Recognition - Search Engine Module

128	IIIT Allahabad	SCL 180 nm	6 Bit ADC & 6 bit DAC
129	NIT Srinagar	SCL 180 nm	ASIC implementation of arbiter unit for NOC
130	CEERI Pilani	SCL 180 nm	Crypto Chip
131	CEERI Pilani	SCL 180 nm	Leon3 based SoC
132	Thapar Institute	SCL 180 nm	Present Cipher Crypto Chip
133	IIT Guwahati	SCL 180 nm	Module for air quality monitoring system
134	IIEST, Shibpur	SCL 180 nm	Single Channel 14 bit Fully Differential SAR ADC
135	IIEST, Shibpur	SCL 180 nm	3-Channel 14 bit Fully Differential SAR ADC
136	Thapar Institute	SCL 180 nm	All-digital 6-bit flash ADC and 4-bit TDC
137	NIT, Arunachal Pradesh	SCL 180 nm	Serializer circuit cum programmable duty cycle generator
138	VNIT Nagpur	SCL 180 nm	Wireless Sensor Network Node for Internet of Things
139	CEERI Pilani	SCL 180 nm	capacitance to digital converter (CDC)
140	CEERI Pilani	SCL 180 nm	Readout Circuits
141	MNNIT Allahabad	SCL 180 nm	LORA Transmitter : 865-867 MHz
142	MNNIT Allahabad	SCL 180 nm	Advance Video Decoder for Mobile Telemedicine(AVDMT)
143	UNIVERSITY OF CALCUTTA	SCL 180 nm	Analog Front End design for differential inductive seismic sensor
144	NIT Goa	SCL 180 nm	5 bit Standard cell based ADC
145	Chip centre, CDAC Bengaluru	SCL 180 nm	SPI based AES Encryptor/Decryptor
146	Chip centre, CDAC Bengaluru	SCL 180 nm	RISC-V Floating point Arithmetic Unit
147	IIT Gandhinagar	SCL 180 nm	Radiation-hard SRAM Memory and Logic Design
148	NIT Durgapur	SCL 180 nm	Analog Front End design for Seismic Application
149	IIT Kharagpur	SCL 180 nm	RF MOM capacitor with 4 metal layer, RF 1:1 Transformer with four metal layer, RF spiral inductor and active image reject filter

150	NIT Durgapur	SCL 180 nm	CMOS Temperature Sensor with built-in ADC
151	SVNIT Surat	SCL 180 nm	Error-Correcting Code (Low Power High Speed Serial Data Transceivers)
152	NIT Jalandhar	SCL 180 nm	Low power RF mixer used in Communication Systems
153	IIT Patna	SCL 180 nm	Single Cycle RISCV - 32I Processor
154	CEERI Pilani	SCL 180 nm	PLL-SRAM Test Chip
154	IIT Kharagpur	SCL 180 nm	Earthquake Early Warning System (EEWS)
155	IIT Kharagpur	SCL 180 nm	Automatic variable gain based AFE for wide range og seismic signal
156	NIT Durgapur	SCL 180 nm	Versatile Data Acquisition & Signal processing platform for Seismic Application
157	NITK Surathkal	SCL 180 nm	Gm-C filter (bandwidth range 5-200 Hz)
158	IIT Bombay	SCL 180 nm	COMPSD_FEB17
159	IIT Guwahati	SCL 180 nm	Signal Conditioning Circuit
160	VNIT Nagpur	SCL 180 nm	CVN-VNIT-C1
161	NIT Patna	SCL 180 nm	Remote Detection of Humans
162	NIT Patna	SCL 180 nm	Speech based person authentication system

Annexure-III

List of IEPs conducted under the SMDP-C2SD Programme

#	Institute	Date	Topic	Faculty/Student Attended
1.	IIT-D	7- 9 Dec' 15	System Level Design on Platform FPGAs	27
2.	IISc-B	4- 8 Jul' 16	Mixed Signal SOC: from design to tape out (.GDS2)	47
3.	IIT-B	11- 13 Jul' 16	Analog, Mixed-Signal and RF System Design	35
4.	VNIT-N	5- 9 Dec' 16	Design issues related to Deep Sub-Micron Technologies	35
5.	IIT-KGP/ IIT-Guwahati	10-14 Apr'17	Introduction to Analog & Digital VLSI Design	22
6.	IIT-KGP/ NIT-Sikkim	5-9 Jun' 17	Mixed Signal and RFIC Design	27
7.	IIT Madras	29Jan - 2 Feb' 18	Analog IC Design	25
8.	IIT Roorkee (with SCL Mohali)	24 - 29 Feb' 18	High Level Design to Silicon	60
9.	IIT Kharagpur	19- 23 Mar'18	IoT for Structural Health Monitoring	30
10.	CDAC Bangalore (Chip Centre)	10-14 June'19	PCB Design methodologies - a hands-on course	28
11.	IISc Bangalore	24-28 June'19	Mixed Signal SoC: from tape out to GDSII	49
12.	NIT Rourkela	1-5th July 19	Design Verification and Hardware Security	18
13.	IIEST Shibpur	26-3 0 Aug 19	Testing and Design-for-Testability for Digital Integrated Circuits	32
14.	NIELIT Calicut (Online training)	05-16 Oct 2020	Embedded System Design on FPGA covering Swadeshi Microprocessors	1000
15.		30 Nov- 12 Dec 2020	Embedded System Design on FPGA covering Swadeshi Microprocessors	450
16.		29th March-02nd April 2021	Learning Management System based Embedded System Design on FPGA "Covering Swadeshi Microprocessors"	106

Annexure-IV

List of Conferences/Workshops supported under SMDP-C2SD programme

Support for attending International Conferences outside the Country

#	Institute Name	Conference Name	Year	Country	Duration
1	IIT Gandhinagar	Radiation and its Effects on Components and Systems (RADECS)	2016	Germany	19th-23th September
2	IIT Hyderabad	International Workshop on Signal Processing Systems(SiPS)	2017	Lorient, France	2nd - 5thOctober
3	Thapar University,Patiala	International Conference on Electrical and Electronics Engineering (ICEEE)	2017	Australia	2nd -3rd February
4	CEERI Pilani	International System-on-Chip Conference	2018	USA	4th -7th September
5	IIT-Bombay	International Symposium on Circuits and Systems (ISCAS)	2018	Florence, Italy	27th - 30th May
6	IIT Mandi	International Symposium on Circuits and Systems (ISCAS)	2018	ITALY	27th-30th May
7	IIT-Guwahati	International Microwave Symposium (IMS)	2019	Boston, USA	2nd -7th June
8	IIT-Bombay	International Symposium on Circuits & Systems (ISCAS)	2019	Japan	26th-29th May
9	Thapar University,Patiala	International Conference on Intelligent Systems (Intellisys)	2019	UK	5th -6th September
10	IIEST Shibpur	International Symposium on Devices, Circuits and Systems (ISDCS)	2019	Japan	6th -8th March
11	NIT Patna	International Symposium on Wireless Per sonal Multimedia Communication (WPMC-2019)	2019	Portugal	24th – 27th November
12	CEERI Pilani	International conference on trust privacy and security in Intelligent System and Application (IEEE TPS-ISA)	2019	California	12th – 14th December

Support for Organizing International Conferences/Workshops in the Country

#	Institute Name	Conference Name	Year	Duration
1	IIT Roorkee	International Symposium on VLSI Design and Test (VDAT)	2017	29th -2nd July
2	C-DAC Bangalore	Analog VLSI & Mixed Signal Design	2017	15th-16th June
3	Thiagarajar College of Engineering, Madurai	International Symposium on VLSI Design and Test (VDAT)	2018	28th -30th June
4	IIT Indore	International Symposium on VLSI Design and Test (VDAT)	2019	4th - 6th July
5	IIT Goa	ARM Architecture and System-on-Chip (SoC) Design	2019	1st-3rd December
6	IIEST Shibpur	International Symposium on Devices, Circuits and System (ISDCS-2020)	2020	4th – 6th January

Annexure-V

List of Patents filed under SMDP-C2SD programme

#	Title	Country	Institute
1	CMOS wideband RF amplifier with gain roll-off compensation for external parasitic	US	IISc Bangalore
2	Methods and apparatus for reduction of motion artifact and noise in ECG signal	India	IIT Bombay
3	Continuously variable precision and linear floating resistor using metal-oxide-semiconductor field-effect transistors	US	IIT Bombay
4	A current source array for high-resolution high-speed digital to Analog converters	India	IIT Gandhinagar
5	A lateral DMOS transistor and method of fabricating thereof	India	IIT Gandhinagar
6	An ultra low power, read decoupled-differential write, 10t sram cell with larger read/write noise margin	India	IIT Indore
7	Offset compensated data sensing technique for low energy embedded RAM	India	IIT Indore
8	On-Chip Jitter measurement circuit for high speed data and clock, high-speed voltage controlled CML hysteresis delay cell and ring oscillator using the same,low power high dynamic range programmable gain amplifier	India	IIT Kharagpur
9	Ultra low trans conductance amplifier using carbon nano tube field effect transistor	India	MNIT Jaipur
10	Power supply noise reduction using clock gating with variable frequency as global clock	India	NIT Agartala
11	N-stage OTA buffer amplifiers with unity gain and high input dynamic range and tunable gain for driving large resistance loads	India	NIT Calicut
12	Internet of things enabled energy management system	India	NIT Hamirpur
13	Method and System for enriching life in a humanly maintained aquaculture environment	India	NIT Hamirpur
14	A novel microfluidic approach for bio-mems applications	India	SVNIT Surat
15	Fully differential clocked comparator for pipelined analog - to - digital converter	India	TIET Patiala
16	A Scalable compact digital-in concept comparator for adc	India	TIET Patiala
17	Polymer electrostatic mems cantilever beam	India	VNIT Nagpur
18	High speed voltage controlled cml hysteresis delay cell and ring oscillator using the same	India	IIT Kharagpur
19	An auxiliary circuit in Analog-to-Digital Converter for adaptive sampling architecture.	India	NIT Goa
20	Amplitude dependent variable sampling frequency based sigma delta modulator	India	NIT Goa
21	Reconfigurable and unified signal processing apparatus for generating variable length Hamming and Hanning window functions	India	NIT, Puducherry